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D-LINK SYSTEMS, INC.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

3COM CORPORATION,

Plaintiff/Counterdefendant,

v.

D-LINK SYSTEMS INC.,

and

REALTEK SEMICONDUCTOR CORPORATION

Defendants/Counterplaintiffs.

Case No. Cv-03-2177-VRW

JOINT CLAIM CONSTRUCTION AND PRE-HEARING STATEMENT PURSUANT TO PATENT LOCAL RULE 4-3

Plaintiff/Counterdefendant 3Com Corporation and Defendants/Counterplaintiffs Realtek Semiconductor Corporation and D-Link Systems Inc., by and through respective counsel, hereby respectfully submit the following Joint Claim Construction and Pre-Hearing Statement pursuant to Patent L.R. 4-3 of the United States District Court for the Northern District of California.

The parties exchanged proposed terms and claim elements for construction pursuant to Patent L.R. 4-1. The parties thereafter exchanged proposed constructions for each term and claim element pursuant to Patent L.R. 4-2 and conducted a meet-and-confer conference regarding the proposed terms and claim elements. The parties expressly reserve their rights to propose constructions of additional terms, phrases or clauses in the asserted patents at a later time. In addition, the parties expressly reserve their rights to supplement or amend the proposed construction and other positions set forth herein.

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I. PATENT L.R. 4-3(a): CLAIM TERMS, PHRASES, OR CLAUSES ON WHICH THE PARTIES AGREE

Pursuant to Patent L.R. 4-3(a), the parties identify those claim terms, phrases, or clauses on which they agree:

A. Claim Terms not Asserted by Parties as Subject to Construction According to 35 U.S.C. § 112 ¶ 6

Claim term	*Joint construction*
"buffer" agreed to with respect to: '625 patent: 23 '884 patent: 1 **The definition of buffer remains in dispute with respect to:** '459 patent: 1 '872 patent: 1, 10, 21 '094 patent: 1, 9, 21, 28, 39, 47	A memory for temporary storage of data
"CSMA/CD" found in claim numbers: '872 patent: 21 '094 patent: 28	A carrier sense multiple access (CSMA) with collision detection (CD) network, such as an Ethernet network
"carrier sense, multiple access network with collision detection" found in claim numbers: '872 patent: 21 '094 patent: 28	A carrier sense multiple access (CSMA) with collision detection (CD) network, such as an Ethernet network
"coupled to the first and second ports" found in claim numbers: '625 patent: 23	connected
"frame(s)" found in claim numbers: '459 patent: 1	A bundle of data in binary form organized in a specific way for transmission

Claim term	*Joint construction*
'872 patent: 1, 10, 21 '094 patent:1, 9, 21, 28, 39, 47	
"in parallel" found in claim numbers: '094 patent: 1, 39	A period of concurrent operation
"medium access controller" found in claim numbers: '872 patent: 21	A device that controls access to the network
"medium access task" found in claim numbers: '094 patent: 39	A task performed by a network interface device for initiating access to a network
"monitoring" found in claim numbers: '094 patent: 9, 21, 28, 39 '872 patent: 1, 10	Watching, keeping track of, or checking on
"network interface adapter" found in claim numbers: '872 patent: 21	Equipment between a computer and a network for enabling communication
"order of receipt" found in claim numbers: '625 patent: 23	The order in which the packets are received by the buffer
"packet filter" found in claim numbers: '884 patent: 1	Hardware and/or software that identifies packets as having variant formats
"port" found in claim numbers: '625 patent: 23 '884 patent: 1	An access point for data entry or exit
"posting status information" found in claim numbers: '872 patent: 10	Storing information about the state of a function or operation

Claim term	*Joint construction*
'094 patent: 21, 47	
"produce a data value dependent on contents of the packet prior to transfer of the identified packets" found in claim numbers: '884 patent: 1	Produce a data value dependent on the contents of the packet before transferring the identified packets to the host
"segmentation circuit" found in claim numbers: '446 patent: 26	Circuitry that generates the frame segment descriptor utilizing the descriptor signal
"threshold determination" found in claim numbers: '872 patent:1, 10, 21 '094 patent: 9, 28, 47	A determination of whether the threshold amount has been reached
"threshold logic" found in claim numbers: '459 patent: 1	Circuits and/or programming that determine(s) whether the threshold value has been reached
"transceiver" found in claim numbers: '459 patent: 1 '872 patent: 10 '094 patent: 28	A device that can both transmit and receive signals
"transfer packets out of the buffer to the other of the first and second ports according to the order of receipt, and according to the respective packet types" found in claim numbers: '625 patent: 23	The order in which packets are transferred out of the buffer is based upon the order in which the packets were received by the buffer and the types of the packets stored in the buffer

II. PATENT L.R. 4-3(b): DISPUTED CLAIM TERMS, PHRASES AND CLAUSES

Pursuant to Patent L.R. 4-3(b), the parties identify the following claim terms, phrases, or clauses on which they disagree, and submit these terms for construction by the Court:

A. Claim Terms not Asserted by Parties as Subject to Construction According to 35 U.S.C. § 112 ¶ 6[1]

1. U.S. Pat. No. 5,307,459

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
"**alterable storage location**" found in claim numbers: '459 patent: 1	PROPOSED CONSTRUCTION: storage location whose value is changeable DICTIONARY/TREATISE DEFINITIONS: alter: The American Heritage Dictionary of the English Language (4th ed. 2000): v. tr. To change or make different; modify: altered my will. intr. To change or become different. INTRINSIC EVIDENCE: Claims: see, e.g., claim 5 (depending from claim 1, claim 5 claiming posting status information which may be used by the host processor as feedback); claim 1; claim 7, claim 22; claim 23; claim 34; claim 35; claim 40; claim 41; claim 44; claim 45; claim 50; claim 51; claim 52; claim 53; Specification: see, e.g., fig. 2, 14-24; col. 2:47-50 ("The threshold logic includes a counter coupled to the buffer memory for counting the data transfer to or from the buffer memory, and an alterable storage location containing a threshold value."); 3:8-14 ("According to another aspect of the present invention, the network interface logic includes	PROPOSED CONSTRUCTION: storage location whose value is dynamically changeable INTRINSIC EVIDENCE: PATENT SPECIFICATION: "If host processor 5 responds to network adapter 3 before a complete data frame is transferred, host processor 5 then may decrease the threshold value in alterable storage location 10a enabling threshold logic 10 to generate the indication signal at a later time in the next transfer of a data frame. Alternatively, if host processor 5 responds to the network adapter 3 after a complete data frame has already been transferred, host processor 5 may then increase the threshold value in alterable storage location 10a enabling the threshold logic to generate an indication signal at an earlier time in the next transfer of a data frame." ('459; Col. 6: 48-59). "The above indication signals are further optimized by allowing the host processor to dynamically tune the timing of the	PROPOSED CONSTRUCTION: storage location whose value is dynamically changeable INTRINSIC EVIDENCE: '459 patent at 42:17-25 ("*The above indication signals are further optimized by allowing the host processor to dynamically tune the timing of the indication signals. The host processor* has write access to the threshold registers and *may alter the threshold values in the threshold registers based on posted status information by the network adapter*. The posted status information will *allow the host processor to determine whether it is responding too early or too late to an interrupt generated by the indications*.") '459 patent at 6:31-59 ("*Threshold logic 10 contains an alterable storage location 10a which contains a threshold value*. This threshold value represents the amount of a data frame which will be transferred into or out of buffer 9 before an early indication signal will be

[1] Defendants contend that "logic" is a signal which invokes 35 U.S.C. § 112 ¶6 in certain asserted claims, while Plaintiff contends that it is an ordinary term. "Logic," and various phrases beginning with that term, are included in this section either because all parties have proposed constructions or because one or more defendants proposed the phrase for construction not under § 112 ¶6 in its 4-1 statement, and because the dispute with respect to whether the term invokes 35 U.S.C. § 112 ¶6 is adequately noted in Sections B and D.

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	control means for generating an interrupt signal to the host processor responsive to the indication signal. The control means also posts status information which may be used by the host processor as feedback for optimizing the threshold value in the alterable storage location."); see also col. 2:50-54; col. 3:18-25; col. 3:37-56; col. 3:67-4:2; col. 4:7-11; col. 6:32-33; col. 6:38-59; col. 23:56-59; col. 29:64-67; col. 30:45-48; col. 31:20-22; col. 42:19-22; Col. 1: 46-51; Col. 1: 63-66; Col. 2: 46-54; Col. 2: 30-35; Col. 2: 23-27; Col. 6: 9-59; Col. 41:44-55; Col. 3:11-14; 42: 17-25; Col. 6: 48-59; Col. 6:31-59 ; Col. 42:17-25; see also Prosecution History: Notice of Allowability, Oct. 14, 1993, pp. 2-3. EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action. See also U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and 6,570,884; Joint Claim Construction Statement in Cv-05-00098 (VRW). 3Com reserves the right to rely on any statement made	indication signals. The host processor has write access to the threshold registers and may alter the threshold values in the threshold registers based on posted status information by the network adapter. The posted status information will allow the host processor to determine whether it is responding too early or too late to an interrupt generated by the indications." ('459; Col. 42: 17-25) (emphasis added). "The control means also posts status information which may be used by the host processor as feedback for optimizing the threshold value in the alterable storage location." ('459; Col. 3: 11-14) (emphasis added). "Threshold logic 10 in network adapter 3 is designed for eliminating or reducing interrupt latency. Threshold logic 10 makes a determination of how much of a data frame is transferred before generating an early indication signal. The early indication signal may then cause an early interrupt signal to be generated during the transfer of a data frame. Moreover, threshold logic 10 is designed such that the time required for transferring the remainder of the data frame should approximately equal the time required for host processor 5 save its system parameters. Therefore, interrupt latency is eliminated or reduced by allowing host processor 5's interrupt routine to coincide	generated which may cause host interface logic 8 to send an interrupt to host processor 5. . . . *The threshold logic also includes a means for the host processor 5 to dynamically alter the time at which an indication is generated based on prior host processor 5 responses*. When responding to an interrupt generated by an early indication, the host processor may examine network adapter status information to determine if host processor 5 is servicing the interrupt too early or too late. If host processor 5 responds to network adapter 3 before a complete data frame is transferred, host processor 5 then may decrease the threshold value in alterable storage location 10a enabling threshold logic 10 to generate the indication signal at a later time in the next transfer of a data frame. Alternatively, if host processor 5 responds to the network adapter 3 after a complete data frame has already been transferred, host processor 5 may then increase the threshold value in alterable storage location 10a enabling the threshold logic to generate an indication signal at an earlier time in the next transfer of a data frame.") '459 patent at 3: 11-14 ("The control means also posts status information which may be used by the host processor as feedback for optimizing the threshold value in the alterable storage

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	by any party under the Patent Local Rules.	with the transfer of the remainder of the data frame. FIG. 2 is a functional block diagram of network adapter 3 with threshold logic 10 illustrating the various transfer paths. Network adapter 3 contains transceiver 12 which transmits and receives data frames across network 2. Network interface logic 11 is responsible for the transfer of a data frame between network buffer 9 and transceiver 12. Likewise, the network adapter 3 contains host interface logic 8 which is responsible for transferring a data frame between network buffer 9 and host system 1. Threshold logic 10 contains an alterable storage location 10a which contains a threshold value. This threshold value represents the amount of a data frame which will be transferred into or out of buffer 9 before an early indication signal will be generated which may cause host interface logic 8 to send an interrupt to host processor 5. Host processor 5 has access to the alterable storage 10a location containing the threshold value through host interface logic 8. The threshold logic also includes a means for the host processor 5 to dynamically alter the time at which an indication is generated based on prior host processor 5 responses. When responding to an interrupt generated by an early indication, the host processor may examine network adapter status information to determine if	location.") '459 patent at 41: 44-55 ("Therefore, the present invention reduces host processor interrupt latency by generating early indications of data frame transfers. These early indications then may be used to generate an early interrupt to the host processor before the data frame is transferred which allows the host processor to save its current environment during a data frame transfer. . . .") DICTIONARY/TREATISE DEFINITIONS: Webster's Ninth New Collegiate Dictionary (Ninth Edition, 1988) Alter: 1: to make different without changing into something else 2: CASTRATE SPAY ~ vi: to become different syn see CHANGE; alterable – adj. EXPERT TESTIMONY: Realtek's expert, Dr. Izhak Rubin, may provide testimony as to the definition of the disputed terms as would be understood by one of ordinary skill in the relevant art and may provide an explanation of the technology.

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		host processor 5 is servicing the interrupt too early or too late. If host processor 5 responds to network adapter 3 before a complete data frame is transferred, host processor 5 then may decrease the threshold value in alterable storage location 10a enabling threshold logic 10 to generate the indication signal at a later time in the next transfer of a data frame. Alternatively, if host processor 5 responds to the network adapter 3 after a complete data frame has already been transferred, host processor 5 may then increase the threshold value in alterable storage location 10a enabling the threshold logic to generate an indication signal at an earlier time in the next transfer of a data frame." ('459; Col. 6: 9-59) (emphasis added). "Therefore, the present invention reduces host processor interrupt latency by generating early indications of data frame transfers. These early indications then may be used to generate an early interrupt to the host processor before the data frame is transferred which allows the host processor to save its current environment during a data frame transfer. The early indications are generated by threshold logic which determines how much of a data frame is transferred before generating an early indication by comparing a threshold value in a threshold register to a data transfer counter." ('459;	

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		Col. 41: 44-55). "Therefore, it is desirable to provide a network adapter with an optimized indication signal to the host processor of the completion of the transfer of a data frame which reduces interrupt latency allowing for optimized network adapter/host system performance." ('459; Col. 2: 23-27). "The present invention provides for optimized indication signals to a host processor by a network adapter of the completion of a transfer of a data frame. The apparatus is coupled between a network transceiver and a host system which includes a host processor and host memory."). "The threshold logic includes a counter coupled to the buffer memory for counting the data transfer to or from the buffer memory, and an alterable storage location containing a threshold value. Means for comparing the counter and the alterable storage location is also provided. The indication signal to the host is generated based on the comparison of the counter and the threshold value in the alterable storage location." ('459; Col. 2: 46-54). "As can be seen, there is interrupt latency between when the network adapter has completed a transfer and when the host processor is able to service the interrupt	

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		generated by the network adapter." ('459; Col. 1: 63-66). "In prior art systems, such as the National Semiconductor DP83932B, a systems-oriented network interface controller (SONIC) and the Intel 82586 local area network co-processor, an interrupt is generated by the network adapter to the host processor on the completion of a data transfer." ('459; Col. 1: 46-51). EXTRINSIC EVIDENCE: *DICTIONARY/TREATISE DEFINITIONS:* Webster's II New College Dictionary (2001), pg. 33: Alterable-"Capable of being changed." *EXPERT TESTIMONY:* D-Link's expert, Howard Frazier, may provide testimony as to the definition of the disputed terms as would be understood by one of ordinary skill in the relevant art and may provide an explanation of the technology. D-Link also incorporates by reference Realtek's references.	
"**buffer**" found in claim numbers: '459 patent: 1 also presented for construction in:	PROPOSED CONSTRUCTION: A memory for temporary storage of data. DICTIONARY/TREATISE DEFINITIONS: The American Heritage Dictionary of the English Language (4th ed. 2000): A device or area	PROPOSED CONSTRUCTION: This term is used only in phrase "buffer memory." See construction of "buffer memory."	Same as "**buffer memory**" identified below.

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
'872 patent: 1, 10, 21 '094 patent: 1, 9, 21, 28, 39, 47	used to store data temporarily; see also Dictionary of Computing (3d ed. 1990): A temporary memory for data, normally used to accommodate the difference in the rate at which two devices can handle data during a transfer; Dictionary of Computing (1st ed. 1983): A temporary memory for data, normally used to accommodate the difference in the rate at which two devices can handle data during a transfer. The buffer may be built into a peripheral device, such as a printer or disk drive, or may be part of the system's main memory; IBM Dictionary of Computing (10th ed. 1993): 1. A routine or storage used to compensate for a difference in rate of flow of data, or time of occurrence of events, when transferring data from one device to another. 4. A portion of storage used to hold input or output data temporarily; Microsoft Computer Dictionary (5th ed. 2002): A region of memory reserved for use as an intermediate repository in which data is temporarily held while waiting to be transferred between two locations or devices; Webster's New World Computer Dictionary (10th ed. 2003): A unit of memory given the task of holding information temporarily, especially while waiting for slower components to catch up. INTRINSIC EVIDENCE: Claims: see, e.g., claim 6; ("the buffer memory comprises a buffer		

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	independent of the host address space"); see also claim 1; claim 2; claim 3; claim 4; claim 11; claim 14; claim 16; claim 18; claim 20; claim 22; claim 24; claim 25; claim 30; claim 32; claim 34; claim 38; claim 39; claim 40; claim 42; claim 43; claim 44; claim 46; claim 47; claim 48; claim 49; claim 50; claim 52; Specification: see, e.g., figs. 2, 6, 7, 9, 11-13 col. 2:38-41 ("The apparatus includes network interface logic for transferring the data frame between the network transceiver and a buffer memory for storing the data frame."); see also col. 1:25-36; col. 1:39-45; col. 2:1-5; col. 2:41-43; col. 2:46-50; col. 2:55-3:7; col. 3:18-22; col. 3:44-46; col. 3:57-67; col. 4:38-48; col. 6:27-32; col. 6:34-38; col. 7:1-2; col. 7:16-20; col. 7:61-63; col. 10:18-25; col. 10:30-32; col. 10:37-40; col. 10:42-45; col. 10:48-51; col. 10:58-61; col. 10:66-68; col. 11:23-26; col. 11:29-36; col. 11:43-47; col. 11:49-52; col. 12:34-37; col. 12:47-49; col. 13:18-21; col. 13:34-41; col. 13:43-49; col. 13:53-56; col. 13:58-68; col. 14:1-4; col. 14:6-21; col. 14:26-29; col. 14:34-40; col. 14:59-62; col. 15:67-16:8; col. 16:15-20; col. 16:34-37; col. 16:43-55; col. 16:61-62; col. 17:5-9; col. 17:41-47; col. 17:52-53; col. 17:55-59; col. 17:61-62; col. 18:4-7; col. 18:23-27; col. 18:30-34; col. 18:47-51; col. 18:62-66; col. 19:2-17; col. 19:19-26; col. 19:28-32; col. 19:49-51; col. 19:60-68; col. 20:16-22; col. 20:45-48; col. 20:55-58; col. 20:60-68; col. 21:1-3;		

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	col. 22:12-14; col. 23:60-64; col. 24:12-15; col. 24:28-30; col. 24:38-44; col. 24:56-59; col. 24:63-68; col. 25:12-19; col. 25:21-24; col. 25:35-41; col. 25:62-63; col. 26:1-3; col. 26:40-42; col. 26:65-67; col. 27:53-55; col. 28:4-6; col. 28:20-22; col. 33:26-33; col. 34:25-28; col. 38:14-17; see also Prosecution History: Notice of Allowability, Oct. 14, 1993, pp. 2-3. EXTRINSIC EVIDENCE: See section I.A, supra (agreed upon definition for "buffer" in '625 and '884 patents). 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action. See also U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and 6,570,884; Joint Claim Construction Statement in Cv-05-00098 (VRW). 3Com reserves the right to rely on any statement made by any party under the Patent Local Rules.		
"**buffer memory**" found in claim numbers: '459 patent: 1 also presented for	PROPOSED CONSTRUCTION: A memory for temporary storage of data. DICTIONARY/TREATISE DEFINITIONS: See "**buffer**" above; memory: Dictionary of Computing (1st ed.	PROPOSED CONSTRUCTION: Dedicated random access memory that (1) stores transmit data, (2) is distinct from a FIFO, (3) can always retransmit a frame of data without having to retrieve it	PROPOSED CONSTRUCTION: A memory that (1) stores frame data such that the frame data can be retrieved independently of the order in which the frame data were stored and the frame data can always be retained

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
construction in: '872 patent: 1, 10, 21 '094 patent: 1, 9, 21, 28, 39, 47	1983): A device or medium that can retain information for subsequent retrieval. The term is synonymous with storage and store, although it is most frequently used for referring to the internal storage of a computer that can be directly addressed by operating instructions; see also The American Heritage Dictionary of the English Language (4th ed. 2000): Computer Science. a. A unit of a computer that preserves data for retrieval. b. Capacity for storing information: two gigabytes of memory. INTRINSIC EVIDENCE: Claims: see, e.g., claim 6; ("the buffer memory comprises a buffer independent of the host address space"); see also claim 1; claim 2; claim 3; claim 4; claim 11; claim 14; claim 16; claim 18; claim 20; claim 22; claim 24; claim 25; claim 30; claim 32; claim 34; claim 38; claim 39; claim 40; claim 42; claim 43; claim 44; claim 46; claim 47; claim 48; claim 49; claim 50; claim 52; Specification: see, e.g., figs. 7-9; col. 2:38-41 ("The apparatus includes network interface logic for transferring the data frame between the network transceiver and a buffer memory for storing the data frame."); see also col. 1:25-36; col. 1:39-45; col. 2:1-5; col. 2:41; col. 2:46-50; col. 2:55-3:7; col. 3:18-22; col. 3:44-46; col. 3:57-67; col. 7:16-19; col. 34:25-28; see also Prosecution History: Notice of Allowability, Oct.	from a host, and (4) controlled independently of the host system. INTRINSIC EVIDENCE: PATENT SPECIFICATION: "The *transmit data buffer* occupies 3K bytes as mentioned above. This region is divided into two 1.5K buffers. Only the data that are downloaded to the adapter via bus master transfers are stored in these buffers. The controller will use both the contents of the transmit data buffer and the immediate data portion of the transmit descriptors, when encapsulating a frame for transmission. The adapter automatically alternates the use of the buffers after choosing the buffer closest to the base of the memory as the power up default." ('459; Col. 13: 59-68) (emphasis added). "Some network adapter interfaces include dedicated *transmit buffers* into which a frame of data composed by the sending system can be downloaded by the sending system. The frame is then stored in the *transmit data buffer* until the media access control functions associated with transmitting the frame on the network have successfully transmitted the frame, or cancelled the frame transmission. If the frame transmission is cancelled, the data may be retained in the *transmit data buffer* until the sending system initiates a second attempt to transmit the frame.	and reused and can be accessed by the host system; and (2) is not a first-in-first-out (FIFO) system. INTRINSIC EVIDENCE: '872 patent at 1:47-54; '094 patent at 1:44-50 ("*Transmit data buffers are to be distinguished from first-in-first-out FIFO systems*, in which the sending system downloads data of a frame into the FIFO, while the network adapter unloads the FIFO during a transmission. *The data in FIFOs cannot be retained and reused by the media access control functions, or by the host, like data in transmit data buffers.*") '872 patent at 1:65-2:2; '094 patent at 1:60-65 ("Furthermore, the prior art systems which use transmit data buffers require the host or sending system to manage the transmit data buffer. A network interface controller transfers data from the host managed transmit data buffer using DMA techniques through a FIFO buffer in the interface controller and on to the network.") '872 patent at 2:7-10; '094 patent at 2:3-5 ("*It is desirable to provide the advantages of a transmit data buffer, while maintaining the communications throughput available from the simpler FIFO based systems.*") '872 patent at 2:35-55; '094 patent at 2:28-52 ("According to another

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	14, 1993, pp. 2-3. EXTRINSIC EVIDENCE: See section I.A, supra (agreed upon definition for "buffer" in '625 and '884 patents); 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action. See also U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and 6,570,884; Joint Claim Construction Statement in Cv-05-00098 (VRW). 3Com reserves the right to rely on any statement made by any party under the Patent Local Rules.	Transmit data buffers are to be distinguished from first-in-first-out FIFO systems, in which the sending system downloads data of a frame into the FIFO, while the network adapter unloads the FIFO during a transmission. The data in FIFOs cannot be retained and reused by the media access control functions, or by the host, like data in *transmit data buffers*." ('872; Col. 1: 36-54) (emphasis added). PROSECUTION HISTORY: The following citation to the prosecution history of the '872 patent supports D-Link's proposed claim construction. During prosecution of the application that issued as the '872 patent, in a Response dated February 23, 1994, 3Com stated the following: "Accordingly, the Firoozmand, et al. reference does not initiate transmission to the network upon the threshold determination. Rather, transmission to the network is initiated only when there is a full frame available in the buffer. When the token has been received by the transmitting station, and it has a full frame for transmission, then a transmission process is begun. The transmission process continues, relying on the threshold determination to keep the pipeline full, only while the token is held by the	aspect of the present invention, the transmit buffer includes a transmit descriptor ring, and a transmit data buffer. . . .") '872 patent at 13:17-48; '094 patent at 12:44-13:5 ("A. Transmit Data Buffer The transmit data buffer occupies 3K bytes as mentioned above. This region is divided into two 1.5K buffers. Only the data that are downloaded to the adapter via bus master transfers are stored in these buffers. The controller will use both the contents of the transmit data buffer and the immediate data portion of the transmit descriptors, when encapsulating a frame for transmission. . . . The transmit buffers are shared by the download DMA logic and the transmit DMA logic. The transmit DMA logic may switch from buffer 0 to buffer 1 and back again freely. The only restriction being the availability of transmit data as defined by the transmit start threshold register. . . .") '872 patent, at 1:5-14 ("CROSS-REFERENCE TO RELATED APPLICATIONS The present application is related to copending U.S. patent application entitled NETWORK INTERFACE WITH HOST INDEPENDENT BUFFER MANAGEMENT, application Ser. No. 07/921,519, filed 28 Jul. 1992, now U.S. Pat. No. 5,299,313, which was

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		transmitting station." "The environment is substantially different from the CSMA/CD network, which begins transmission to the medium access controller as soon as the threshold determination is met for an incoming frame. The MAC may succeed in transmitting the frame, may suffer collisions, or may suffer other types of errors which require backoff. Thus, the adapter as claimed in new claims 24-29, initiates transmission without being assured that the medium access controller is able to gain access to the communications medium. *This is a much more sophisticated control environment than that required by the FDDI system of Firoozmand, et al."* Response dated February 23, 1994, p. 5. EXTRINSIC EVIDENCE: *PRIOR ART:* <u>Datesheet for "82596CA High-Performance 32-Bit Local Area Network Coprocessor,"</u> November 1989, Intel Corp (Disclosed in D-Link's Preliminary Infringement Contentions), pg. 2: "Two large, independent FIFOs-128 bytes for Receive and 64 bytes for Transmit-tolerate long bus latencies and provide programmable thresholds that allow the user to optimize bus overhead for any worst-case	owned at the time of invention and is currently owned by the same assignee.") '459 patent, at 1:5-13 ("CROSS-REFERENCE TO RELATED APPLICATIONS The present application is related to copending U.S. patent application entitled NETWORK INTERFACE WITH HOST INDEPENDENT BUFFER MANAGEMENT, Ser. No. 07/921,519, filed Jul. 28, 1992, which was owned at the time of invention and is currently owned by the same assignee.") '459 patent, at 13:58-14:22 ("A. Transmit Data Buffer The transmit data buffer occupies 3K bytes as mentioned above. This region is divided into two 1.5K buffers. Only the data that are downloaded to the adapter via bus master transfers are stored in these buffers. The controller will use both the contents of the transmit data buffer and the immediate data portion of the transmit descriptors, when encapsulating a frame for transmission. . . . The transmit buffers are shared by the download DMA logic and the transmit DMA logic. The transmit DMA logic may switch from buffer 0 to buffer 1 and back again freely. The only restriction being the availability of transmit data as defined by the transmit start threshold register. The transmit DMA module switches from one buffer to

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		bus latency." Datasheet for "The SUPERNET 2 Family for FDDI", October 1991, Advanced Micro Devices, Inc. (Disclosed in D-Link's Preliminary Infringement Contentions), pg. 2-37 : "The transmit FIFO (Figure 1) is a 36-bit by 9-word first-in-first-out register that temporarily stores data to be transmitted. In this way, continuity of data transmission is assured by providing a way to store a portion of the output data stream to compensate for delays involved in accessing the buffer memory." 1992 Local Area Network Databook Including Datasheet For DP83932B Systems-Oriented Network Interface Controller (SONIC), 1992, National Semiconductor Corp, pg.1-295: "The SONIC incorporates two independent 32-byte FIFOs for transferring data to/from the system interface and from/to the network. The FIFOs, providing temporary storage of data, free the host system from the real-time demands on the network." *DICTIONARY/TREATISE DEFINITIONS:* McGraw-Hill Illustrated Telecom Dictionary, Fourth Edition, 2001, pg. 83: Buffer - "A temporary storage (memory) device for data. A buffer is basically a box with RAM inside it. A common application for buffers is to collect a stream	the other whenever it has completed a transmission. The buffer switch occurs regardless of whether or not the transmission was successful and regardless of whether or not bus master download data were used in the preceding transmission. . . . ") DICTIONARY/TREATISE DEFINITIONS: The Network Interface Technical Guide, (First Edition, 1992) Buffer: A temporary storage area in random access memory where the NIC or computer stores information (usually while transmitting or receiving network traffic). EXPERT TESTIMONY: Realtek's expert, Dr. Izhak Rubin, may provide testimony as to the definition of the disputed terms as would be understood by one of ordinary skill in the relevant art and may provide an explanation of the technology. PRIOR ART: Datesheet for "82596CA High-Performance 32-Bit Local Area Network Coprocessor," November 1989, Intel Corp, pg. 2 ("Two large, independent FIFOs-128 bytes for Receive and 64 bytes for Transmit-tolerate long bus latencies and provide programmable thresholds that allow the user to optimize bus overhead for

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		of data and temporarily store it until another device, such as a PC or server asks the buffer to download it. This is useful when the PC, server or LAN could be out of service for a period of time. When the server or PC is returned to service it just asks for the data from the buffer and it is downloaded. The buffer is then empty and ready to receive more data." *EXPERT TESTIMONY:* D-Link's expert, Howard Frazier, may provide testimony as to the definition of the disputed terms as would be understood by one of ordinary skill in the relevant art and may provide an explanation of the technology. D-Link also incorporates by reference Realtek's cited references.	any worst-case bus latency.") Datasheet for "The SUPERNET 2 Family for FDDI", October 1991, Advanced Micro Devices, Inc., pg. 2-37 ("The transmit FIFO (Figure 1) is a 36-bit by 9-word first-in-first-out register that temporarily stores data to be transmitted. In this way, continuity of data transmission is assured by providing a way to store a portion of the output data stream to compensate for delays involved in accessing the buffer memory.") 1992 Local Area Network Databook Including Datasheet For DP83932B Systems-Oriented Network Interface Controller (SONIC), 1992, National Semiconductor Corp, pg.1-295: ("The SONIC incorporates two independent 32-byte FIFOs for transferring data to/from the system interface and from/to the network. The FIFOs, providing temporary storage of data, free the host system from the real-time demands on the network.") Ethernet/IEEE-802.3 Family 1990 World Network Data Book/Handbook, Advanced Micro Devices, pg. 1-63, ("FIFO Operations The FIFO provides temporary buffer storage for data being transferred between the parallel bus I/O pins and serial bus I/O pins. The capacity of the FIFO is 48 bytes.

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
			Transmit Data is loaded into the FIFO under internal micro-program control. The FIFO must be more than 16 bytes empty before the ILACC requests the bus (HOLD/BURREQ is asserted). The ILACC will start sending the preamble (if the line is idle) as soon as there is one byte loaded into the FIFO. Should the transmitter be required to back off, there will be up to 32 bytes of data in the FIFO ready for transmission. Reception has priority over transmission during the time that the transmitter is backing off. Receive Data is loaded into the FIFO from the serial input shift register during reception and leaves the FIFO under microprogram control. The ILACC microcode will wait until there are at least 16 bytes of data in the FIFO before initiating a DMA burst transfer. Preamble (including the synchronization bits) is not loaded into the FIFO.")
"**host system**" found in claim numbers: '459 patent: 1 also presented for construction in: '872 patent: 1, 10, 21 '094 patent: 1, 9, 21, 28, 39, 47	PROPOSED CONSTRUCTION: A computer that communicates over a network DICTIONARY/TREATISE DEFINITIONS: Webster's New World Computer Dictionary (10th ed. 2003): 1. In the Internet, any computer that can function as the beginning and end point of data transfers. An Internet	PROPOSED CONSTRUCTION: Any system or computer that communicates over a network INTRINSIC EVIDENCE (872: Col 1: lns. 65-67) (094: Col. 1, lns. 60-62) Furthermore, the prior art systems which use transmit data buffers require the *host or sending system* to	PROPOSED CONSTRUCTION: Any system or computer that communicates over a network Evidence (872: Col 1: lns. 65-67) (094: Col. 1, lns. 60-62) Furthermore, the prior art systems which use transmit data buffers require the *host or sending system* to

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
'884 patent: 1	host has a unique Internet address (called an IP address) and a unique domain name. 2. In networks and telecommunications generally, a server that performs centralized functions, such as making program or data files available to other computers; The American Heritage Dictionary of the English Language (4th ed. 2000): Computer Science. A computer containing data or programs that another computer can access by means of a network or modem; Dictionary of Computing (3d ed. 1990): Host computer (host): A computer that is attached to a network and provides services other than simply acting as a store-and-forward processor or communication switch. INTRINSIC EVIDENCE: Claims: claim 1; claim 3; claim 4; claim 5; claim 6; claim 11; claim 16; claim 18; claim 22; claim 23; claim 24; claim 25; claim 30; claim 34; claim 35; claim 38; claim 39; claim 40; claim 41; claim 42; claim 44; claim 45; claim 46; claim 47; claim 48; claim 50; claim 51; claim 52; claim 53; Specification: see, e.g., col. col. 5:66-68 ("The host system further includes host memory 6, host processor 5, and other host devices 7 coupled to host bus 4."); see also col. 1:20-23; col. 1:23-25; col. 1:25-31; col. 1:31-37; col. 1:37-38; col. 1:38-42; col.	manage the transmit data buffer. (872: Col. 3, ln. 65 to col. 4., ln. 2) ('094: Col. 3, lns. 59-64) As shown in FIG. 1, such system for communicating data includes a host data processing system, generally referred to by reference number 1, which includes a host system bus 2, a host central processing unit 3, host memory 4, and other host devices 5, all communicating across the bus 2	manage the transmit data buffer. (872: Col. 3, ln. 65 to col. 4., ln. 2) ('094: Col. 3, lns. 59-64) As shown in FIG. 1, such system for communicating data includes a host data processing system, generally referred to by reference number 1, which includes a host system bus 2, a host central processing unit 3, host memory 4, and other host devices 5, all communicating across the bus 2 (884: Col. 2, lns. 39-44) The invention is particularly suited to environments in which the host system is actively handling communications and other processing tasks, and in which the adapter is able to take over some specialized tasks without interfering with the active processing in the host system.

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	1:42-46; col. 1:46-51; col. 1:51-54; col. 1:54-56; col. 1:56-59; col. 1:59-63; col. 1:63-66; col. 1-2:66-1; col. 2:1-6; col. 2:6-8; col. 2:8-13; col. 2:18-22; col. 2:22-28; col. 2:30-32; col. 2:32-35; col. 2:35-37; col. 2:37-38; col. 2:41-43; col. 2:43-46; col. 2:52-55; col. 2:55-59; col. 2:59-63; col. 2:63-67; col. 2-3:67-2; col. 3:8-11; col. 3:11-15; col. 3:25-28; col. 3:28-33; col. 3:44-47; col. 3:61-65; col. 3:65-67; col. 4:21-24; col. 4:28-31; col. 4:31-34; col. 4:34-36; col. 4:45-49; col. 5:56-58; col. 5:58-60; col. 5:61-62; col. 5:62-64; col. 5:64-66; col. 5:66-68; col. 6:2-5; col. 6:5-9; col. 6:15-19; col. 6:19-23; col. 6:29-32; col. 6:34-38; col. 6:38-41; col. 6:41-44; col. 6:44-48; col. 6:48-53; col. 6:53-60; col. 6:61-63; col. 7:9-12; col. 7:16-19; col. 7:21-23; col. 7:54-56; col. 7:61-63; col. 8:8-11; col. 8:46; col. 9:20-24; col. 9:24-27; col. 9:34-36; col. 9:38-43; col. 9:57-59; col. 10:5-8; col. 10:16-18; col. 10:25-30; col. 11:29-33; col. 11:36-40; col. 11:43-45; col. 11:52-56; col. 11:56-60; col. 11:60-64; col. 11:64-66; col. 12:4-7; col. 12:18-22; col. 12:22-24; col. 12:24-58; col. 12:58-29; col. 12:29-30; col. 12:30-33; col. 12:39-43; col. 12:43-47; col. 12:47-50; col. 12:58-60; col. 12:60-66; col. 12:66-67; col. 12-13:67-3; col. 13:8-12; col. 13:12-14; col. 13:14-16; col. 13:16-18; col. 13:25-26; col. 13:34-37; col. 13:37-42; col. 13:42-43; col. 14:32-34; col. 14:41-46; col. 14:46-48; col. 15:4-7; col. 15:10-12; col. 15:23-27; col. 15:30-32; col. 15:36-39; col. 15:39-42;		

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	col. 15:42-45; col. 15:52-55; col. 15:61-62; col. 15:62-67; col. 15:67-1; col. 16:1-3; col. 16:3-6; col. 16:9-13; col. 16:13-15; col. 16:16-19; col. 16:22-24; col. 16:34-37; col. 16:37-40; col. 16:43-45; col. 16:47-48; col. 17:1-4; col. 17:12-15; col. 17:33-35; col. 17:45-47; col. 17:52-53; col. 17:55-58; col. 18:4-7; col. 18:7-9; col. 18:9-17; col. 18:19-22; col. 18:24-27; col. 18:27-29; col. 18:30-35; col. 18:47-51; col. 18:51-53; col. 18:53-56; col. 18:56-58; col. 18:58-62; col. 18:62-66; col. 19:9-14; col. 19:29-34; col. 19:34-36; col. 19:36-42; col. 19:46-47; col. 19:47-49; col. 19:52-55; col. 19:64-66; col. 20:1-5; col. 20:13-16; col. 20:16-24; col. 20:37-40; col. 20:43-45; col. 20:49-53; col. 21:4-8; col. 21:9-11; col. 21:11-16; col. 21:16-18; col. 21:22-25; col. 21:40-42; col. 22:18-23; col. 22:49-52; col. 23:6-9; col. 23:30-33; col. 23:37-39; col. 23:43-47; col. 23:60-64; col. 24:17-19; col. 24:19-22; col. 24:31-34; col. 24:34-37; col. 24:38-40; col. 24:48-51; col. 24:51-52; col. 24:63-1; col. 25:1-2; col. 25:2-6; col. 25:6-7; col. 25:28-31; col. 25:31-33; col. 25:53-55; col. 25:55-56; col. 25:56-57; col. 25:57-60; col. 25:62-65; col. 25:65-1; col. 26:18-21; col. 26:22-23; col. 26:25-26; col. 26:27-29; col. 26:29-32; col. 26:32-35; col. 26:37-39; col. 26:40-43; col. 27:16-17; col. 27:22-26; col. 27:45-47; col. 27:47-52; col. 27:52-55; col. 27:55-60; col. 28:7-9; col. 28:11-13; col. 28:17-20; col. 28:22-24; col. 28:24-26; col. 28:27-30; col. 28:31-33; col. 28:42-46; col. 29:9-12; col. 29:12-15; col. 29:23-25; col. 30:10-13; col.		

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	30:44-47; col. 30:47-48; col. 30:48-51; col. 30:51-55; col. 30:55-57; col. 30:64-67; col. 32:13-15; col. 32:39-44; col. 32:62-65; col. 32:65-68; col. 33:9-12; col. 33:12-15; col. 33:28-33; col. 33:33-40; col. 33:40-46; col. 33:46-49; col. 34:20-22; col. 34:25-28; col. 34:28-31; col. 34:38-41; col. 34:43-46; col. 34:46-50; col. 34:50-52; col. 35:36-38; col. 35:38-41; col. 35:44-46; col. 35:51-53; col. 36:40-42; col. 36:44-46; col. 38:12-14; col. 39:31-38; col. 39-40:67-3; col. 41:34-40; col. 41:44-46; col. 41:46-51; col. 42:6-11; col. 42:17-19; col. 42:19-22; col. 42:22-25; see also Prosecution History: Notice of Allowability, Oct. 14, 1993, pp. 2-3. EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action. See also U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and 6,570,884; Joint Claim Construction Statement in Cv-05-00098 (VRW). 3Com reserves the right to rely on any statement made by any party under the Patent Local Rules.		
"**indication signal**" found in claim	PROPOSED CONSTRUCTION: A signal that indicates a subsequent action, such as	PROPOSED CONSTRUCTION: A signal that indicates the timing for a subsequent	PROPOSED CONSTRUCTION: A signal that is not an interrupt but may be used by

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
numbers: '459 patent: 1	an interrupt DICTIONARY/TREATISE DEFINITIONS: indication: The American Heritage Dictionary of the English Language (4th ed. 2000): Something that serves to indicate; a sign; signal: The American Heritage Dictionary of the English Language (4th ed. 2000): An indicator, such as a gesture or colored light, that serves as a means of communication. Electronics. An impulse or a fluctuating electric quantity, such as voltage, current, or electric field strength, whose variations represent coded information. The sound, image, or message transmitted or received in telegraphy, telephony, radio, television, or radar; see also Dictionary of Computing (1st ed. 1983):Indicator: A bit or bit configuration that may be inspected to determine a status or condition; IBM Dictionary of Computing (10th ed. 1993): Indicator: A device that gives a visual or other indication of the existence of a defined state; Dictionary of Computing (3d ed. 1990): Indicator: A bit or bit configuration that may be inspected to determine a status or condition. INTRINSIC EVIDENCE: Claims: see, e.g., claim 12 ("the indication signal includes an early receive signal"); see also claim 1; claim 5; claim 13; claim 17; claim 19; claim 21; claim 22; claim 23; claim 31; claim 34; claim 35; claim	action, such as an interrupt REFERENCES: PATENT SPECIFICATION: Optimized indication signals of a completed data frame transfer are generated by a network adapter which reduces host processor interrupt latency. The network adapter comprises network interface logic for transferring the data frame between the network and a buffer memory and host interface logic for transferring the data frame between the buffer memory and the host system. The network adapter further includes threshold logic where a threshold value in an alterable storage location is compared to a data transfer counter in order to generate an early indication signal. The early indication signal may be used to generate an early interrupt signal to a host processor before a transfer of a data frame is completed." ('459, Abstract). "Network adapters involved in the transfer of data frames between a communications network and a host computer system typically notify the host processor of the completion of a data frame transfer. In many circumstances, the host processor must take some action based on a completed transfer of a data frame. For example, if the network adapter has received a data frame, the host processor may need to view the data frame resident	the host system to generate an interrupt. INTRINSIC EVIDENCE: '459 patent, Abstract ("*Optimized indication signals of a completed data frame transfer are generated by a network adapter which reduces host processor interrupt latency.* . . . The network adapter further includes threshold logic where a threshold value in an alterable storage location is compared to a data transfer counter in order to generate an early indication signal. *The early indication signal may be used to generate an early interrupt signal to a host processor* before a transfer of a data frame is completed. . . . ") '459 patent at 1:20-2:27("2. Description of Related Art Network adapters involved in the transfer of data frames between a communications network and a host computer system typically notify the host processor of the completion of a data frame transfer. In many circumstances, the host processor must take some action based on a completed transfer of a data frame. For example, if the network adapter has received a data frame, the host processor may need to view the data frame resident in the network adapter buffer memory before allowing transfer of the data frame to host memory or other host devices on the computer system bus.

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	40; claim 41; claim 44; claim 45; claim 50; claim 51; claim 52; claim 53; Specification: see, e.g., col. 2:35-38 ("The apparatus is coupled between a network transceiver and a host system which includes a host processor and host memory.");col. 2:52-54 ("The indication signal to the host is generated based on the comparison of the counter and the threshold value in the alterable storage location"); col. 3:7-11 ("According to another aspect of the present invention, the network interface logic includes control means for generating an interrupt signal to the host processor responsive to the indication signal."); col. 3:33-4:12 ("According to yet another aspect of the present invention, the network adapter includes look-ahead threshold logic for generating an early receive indication signal during the receiving of the data frame. The data frame includes a header field followed by a data field. The look-ahead threshold logic includes an alterable storage location containing a look-ahead threshold value representing an amount of data relative to the beginning of the header field. A comparison between the look-ahead threshold value in the alterable storage location and the counter generates an early receive indication signal. View logic is also provided to present the data frame in the buffer memory to the host system prior to transferring to the host	in the network adapter buffer memory before allowing transfer of the data frame to host memory or other host devices on the computer system bus. Moreover, if a determination is made that the data frame will be transferred to the host computer system, *the host processor may require notification of the completion of the transfer of the data frame* from the network adapter buffer memory to the host computer system. "Likewise, with respect to the transmission path, the host processor may require notification on the completion of a data frame transfer. The host processor may require notification of the completion of a download of a data frame from a host system to the network adapter buffer memory. In addition, a notification to the host processor on the completion of the transmission of a data frame from the network adapter buffer memory onto the communications network may be required. "In prior art systems, such as the National Semiconductor DP83932B, a systems-oriented network interface controller (SONIC) and the Intel 82586 local area network co-processor, *an interrupt is generated by the network adapter to the host processor on the completion of a data transfer.* The host processor then must determine the cause of the	Moreover, if a determination is made that the data frame will be transferred to the host computer system, *the host processor may require notification of the completion of the transfer of the data frame* from the network adapter buffer memory to the host computer system. Likewise, with respect to the transmission path, the host processor may require notification on the completion of a data frame transfer. The host processor may require notification of the completion of a download of a data frame from a host system to the network adapter buffer memory. In addition, a notification to the host processor on the completion of the transmission of a data frame from the network adapter buffer memory onto the communications network may be required. *In prior art systems*, such as the National Semiconductor DP83932B, a systems-oriented network interface controller (SONIC) and the Intel 82586 local area network co-processor, *an interrupt is generated by the network adapter to the host processor on the completion of a data transfer.* The host processor then must determine the cause of the interrupt by examining the appropriate network adapter status registers and take the appropriate action. However, before the host processor services the interrupt, the host processor

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	memory. Yet, according to another aspect of the present invention, the network adapter includes length-left threshold logic for generating a receive complete indication signal during the receiving of the data frame which includes a header field followed by a data field. The length-left threshold includes an alterable storage location containing a length-left threshold value representing an amount of data relative to the end of the data field. A comparison of the length-left threshold value in the alterable storage location and the counter generates an early receive indication signal. Also, error detection means is provided for checking the data field transferred from the network transceiver to the buffer memory which generates a receive frame status signal. According to another aspect of the present invention, the network adapter includes transfer threshold logic for generating a transfer complete indication signal during the transferring of the data frame from the network buffer memory to the host system. The network buffer memory being independent from the host address space. The transfer threshold logic includes an alterable storage location containing a transfer threshold value representing an amount of the data frame to be transferred before generating a transfer complete indication."); see also col. 1:20-2:27; col.	interrupt by examining the appropriate network adapter status registers and take the appropriate action. However, before the host processor services the interrupt, the host processor must save its current environment or system parameters. This routine of saving the host processor's current environment may take as long as 30 .mu.s for a OS/2 operating system. The period of time necessary for saving the host processor's environment depends upon the type of host processor used, the host computer system configuration and when the interrupt /occurred. "As can be seen, *there is interrupt latency between when the network adapter has completed a transfer and when the host processor is able to service the interrupt generated by the network adapter.* In essence, the host system/network adapter performance is in an idle state even though a transfer has been completed because the host processor is saving its current environment. For example, a data frame may have been received and is resident in the network adapter buffer memory for as long as 30 .mu.s before the host processor is able to determine the cause of the interrupt and view the data frame. "The host system/network adapter performance degradation introduced by interrupt latency is	must save its current environment or system parameters. This routine of saving the host processor's current environment may take as long as 30 .µs for a OS/2 operating system. The period of time necessary for saving the host processor's environment depends upon the type of host processor used, the host computer system configuration and when the interrupt /occurred. *As can be seen, there is interrupt latency between when the network adapter has completed a transfer and when the host processor is able to service the interrupt generated by the network adapter.* In essence, the host system/network adapter performance is in an idle state even though a transfer has been completed because the host processor is saving its current environment. For example, a data frame may have been received and is resident in the network adapter buffer memory for as long as 30 µs before the host processor is able to determine the cause of the interrupt and view the data frame. The host system/network adapter performance degradation introduced by interrupt latency is compounded when multiple data frames are transferred. Between each data frame transfer, there will be an embedded delay period when the network adapter is waiting for the host processor to save its current environment and respond to

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	41:44-50; col. 42:17-25; col. 2:29-41; col. 6:9-59; col. 5:68-6:22; col. 2:22-26; col. 2:30-39; col. 2:43-50; col. 3:8-11; col. 3:15-18; col. 3:22-36; col. 3:41-43; col. 3:47-51; col. 3:54-57; col. 3:61-65; col. 4:3-7; col. 6:10-15; col. 6:34-40; col. 6:48-60; col. 29:31-39; col. 29:64-66; col. 30:10-13; col. 34:26-28; col. 42:17-19; see also Prosecution History: Notice of Allowability, Oct. 14, 1993, pp. 2-3. EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action. See also U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and 6,570,884; Joint Claim Construction Statement in Cv-05-00098 (VRW). 3Com reserves the right to rely on any statement made by any party under the Patent Local Rules.	compounded when multiple data frames are transferred. Between each data frame transfer, there will be an embedded delay period when the network adapter is waiting for the host processor to save its current environment and respond to a network adapter interrupt signal. "Performance degradation is further complicated by the dynamic nature of interrupt latency. While interrupt latency is relatively constant given a periodic interrupt, interrupt latency may increase substantially in the form of spikes depending upon when the interrupt occurred. Moreover, the host computer system configuration may be altered by installation of additional software or devices on the system bus which will increase interrupt latency. "Therefore, it is desirable to provide a network adapter with an optimized indication signal to the host processor of the completion of the transfer of a data frame *which reduces interrupt latency allowing* for optimized network adapter/host system performance." ('459 col.1:20-2:27). "The present invention provides for optimized indication signals to a host processor by a network adapter of the completion of a transfer of a data frame. The apparatus is coupled between a network transceiver and a host	a network adapter interrupt signal. Performance degradation is further complicated by the dynamic nature of interrupt latency. While interrupt latency is relatively constant given a periodic interrupt, interrupt latency may increase substantially in the form of spikes depending upon when the interrupt occurred. Moreover, the host computer system configuration may be altered by installation of additional software or devices on the system bus which will increase interrupt latency. *Therefore, it is desirable to provide a network adapter with an optimized indication signal to the host processor of the completion of the transfer of a data frame which reduces interrupt latency allowing for optimized network adapter/host system performance.*") '459 patent at 2:29-41 ("The present invention provides for optimized indication signals to a host processor by a network adapter of the completion of a transfer of a data frame. The apparatus is coupled between a network transceiver and a host system which includes a host processor and host memory. The apparatus generates an indication signal to the host processor responsive to the transfer of a data frame. The host processor responds to the indication signal after a period of time. The

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		system which includes a host processor and host memory. The apparatus generates an indication signal to the host processor responsive to the transfer of a data frame. The host processor responds to the indication signal after a period of time. The apparatus includes network interface logic for transferring the data frame between the network transceiver and a buffer memory for storing the data frame." ('459 col. 2:29-41) "Typically, devices on host bus 4, such as network adapter 3, request service from host processor 5 by generating an interrupt on host bus 4. The host processor 5 then must save its system parameters and determine which device caused the interrupt and what service is required. Interrupt latency is introduced from when a device such as network adapter 3 generates an interrupt signal and when host processor 5 is able to service the device. "Threshold logic 10 in network adapter 3 is designed for eliminating or reducing interrupt latency. Threshold logic 10 makes a determination of how much of a data frame is transferred before generating an early indication signal. The early indication signal may then cause an early interrupt signal to be generated during the transfer of a data frame. Moreover, threshold logic 10 is designed such	apparatus includes network interface logic for transferring the data frame between the network transceiver and a buffer memory for storing the data frame.") '459 patent at 6:9-59 ("Threshold logic 10 in network adapter 3 is designed for eliminating or reducing interrupt latency. Threshold logic 10 makes a determination of how much of a data frame is transferred before generating an early indication signal. *The early indication signal may then cause an early interrupt signal to be generated during the transfer of a data frame.* Moreover, threshold logic 10 is designed such that the time required for transferring the remainder of the data frame should approximately equal the time required for host processor 5 save its system parameters. Therefore, interrupt latency is eliminated or reduced by allowing host processor 5's interrupt routine to coincide with the transfer of the remainder of the data frame. FIG. 2 is a functional block diagram of network adapter 3 with threshold logic 10 illustrating the various transfer paths. Network adapter 3 contains transceiver 12 which transmits and receives data frames across network 2. Network interface logic 11 is responsible for the transfer of a data frame between network buffer 9 and transceiver 12.

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		that the time required for transferring the remainder of the data frame should approximately equal the time required for host processor 5 save its system parameters. Therefore, interrupt latency is eliminated or reduced by allowing host processor 5's interrupt routine to coincide with the transfer of the remainder of the data frame." ('459 col. 5:68-6:22). "Therefore, the present invention reduces host processor interrupt latency by generating early indications of data frame transfers. These early indications then may be used to generate an early interrupt to the host processor before the data frame is transferred which allows the host processor to save its current environment during a data frame transfer." ('459, col. 41:44-50). "The above indication signals are further optimized by allowing the host processor to dynamically tune the timing of the indication signals. The host processor has write access to the threshold registers and may alter the threshold values in the threshold registers based on posted status information by the network adapter. The posted status information will allow the host processor to determine whether it is responding too early or too late to *an interrupt generated by the indications*." ('459, col.	Likewise, the network adapter 3 contains host interface logic 8 which is responsible for transferring a data frame between network buffer 9 and host system 1. Threshold logic 10 contains an alterable storage location 10a which contains a threshold value. This threshold value represents the amount of a data frame which will be transferred into or out of buffer 9 before an early indication signal will be generated which may cause host interface logic 8 to send an interrupt to host processor 5. Host processor 5 has access to the alterable storage 10a location containing the threshold value through host interface logic 8. The threshold logic also includes a means for the host processor 5 to dynamically alter the time at which an indication is generated based on prior host processor 5 responses. When responding to an interrupt generated by an early indication, the host processor may examine network adapter status information to determine if host processor 5 is servicing the interrupt too early or too late. If host processor 5 responds to network adapter 3 before a complete data frame is transferred, host processor 5 then may decrease the threshold value in alterable storage location 10a enabling threshold logic 10 to generate the indication signal at a later time in the next transfer of a data frame. Alternatively, if host

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		42:17-25, emphasis added.) *DICTIONARY/TREATISE DEFINITIONS:* <u>Webster's Third New International Dictionary Unabridged (1981):</u> something (as a signal …) that serves to indicate *EXPERT TESTIMONY:* D-Link's expert, Howard Frazier, may provide testimony as to the definition of the disputed terms as would be understood by one of ordinary skill in the relevant art and may provide an explanation of the technology. D-Link also incorporates by reference Realtek's cited references.	processor 5 responds to the network adapter 3 after a complete data frame has already been transferred, host processor 5 may then increase the threshold value in alterable storage location 10a enabling the threshold logic to generate an indication signal at an earlier time in the next transfer of a data frame.") '459 patent at 5:68-6:22 ("Typically, devices on host bus 4, such as network adapter 3, request service from host processor 5 by generating an interrupt on host bus 4. The host processor 5 then must save its system parameters and determine which device caused the interrupt and what service is required. Interrupt latency is introduced from when a device such as network adapter 3 generates an interrupt signal and when host processor 5 is able to service the device. Threshold logic 10 in network adapter 3 is designed for eliminating or reducing interrupt latency. Threshold logic 10 makes a determination of how much of a data frame is transferred before generating an early indication signal. The early indication signal may then cause an early interrupt signal to be generated during the transfer of a data frame. Moreover, threshold logic 10 is designed such that the time required for transferring the remainder of the data frame should approximately equal the

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			time required for host processor 5 save its system parameters. Therefore, interrupt latency is eliminated or reduced by allowing host processor 5's interrupt routine to coincide with the transfer of the remainder of the data frame.") '459 patent; at 41:44-50 ("Therefore, the present invention reduces host processor interrupt latency by generating early indications of data frame transfers. These early indications then may be used to generate an early interrupt to the host processor before the data frame is transferred which allows the host processor to save its current environment during a data frame transfer.") DICTIONARY/TREATISE DEFINITIONS: signal Newton's' Telecom Dictionary (fourth edition, 1991) Signal: 1. An electrical wave used to convey information 2. An alert. 3. An acoustic device (e.g. a bell) or a visual device (e.g. a lamp) which calls attention. To transmit an information signal or alerting signal. McGraw Hill Electronics Dictionary (fifth edition, 1994) Signal: Any variation in an electrical current, visible or nonvisible light, audible or ultrasonic energy that

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			conveys information. Signals can be coded in frequency, phase, or amplitude to separate them from unwanted noise. EXPERT TESTIMONY: Realtek's expert, Dr. Izhak Rubin, may provide testimony as to the definition of the disputed terms as would be understood by one of ordinary skill in the relevant art and may provide an explanation of the technology.
"**logic**" found in claim numbers: '459 patent: 1 also presented for construction in: '872 patent: 1, 21 '625 patent: 23 '884 patent: 1	PROPOSED CONSTRUCTION: Circuitry and/or programming. DICTIONARY/TREATISE DEFINITIONS: Synopsis, Inc., Electronic Design Automation Glossary of Terms, *at* http://www.synopsis.com/news/pr_kit/eda_glossry.html: The sequence of functions performed by hardware or software. Hardware logic is made up of circuits that perform an operation. Software logic is the sequence of instructions in a program; see also IBM Dictionary of Computing (10th ed. 1993): The systematized interconnection of digital switching functions, circuits, or devices; Microsoft Computer Dictionary (5th ed. 2002): In programming, the assertions, assumptions, and operations that define what a given program does. Defining the logic of a program is often the first step in developing the	PROPOSED CONSTRUCTION: When used as a standalone term in the claims, "logic" is an unspecified claim element defined only by its function and thus requires interpretation under invokes 35 U.S.C. § 112 ¶ 6. In computer software or hardware context, "means" or "means for." See discussion in section below concerning 35 U.S.C. § 112 ¶ 6 constructions for phrases including "logic." D-Link also incorporates by reference Realtek's references.	Please refer to the construction under 35 U.S.C. § 112 ¶ 6 for the separate claim limitations of the separate claims. To the extent this term requires construction, Realtek asserts that "logic" (or "logic for") should be construed as "means" (or "means for") and, therefore, the associated claim elements should be governed by 35 U.S.C. § 112 ¶ 6. If the Court determines that 35 U.S.C. § 112 ¶ 6 does not apply, "logic" should be construed as "device." DICTIONARY/TREATISE DEFINITIONS: Synopsis, Inc., Electronic Design Automation Glossary of Terms The sequence of functions performed by hardware or software. Hardware logic is made up of circuits that perform an operation. Software logic is the sequence of instructions in a program.

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	program's source code. INTRINSIC EVIDENCE: Claims: claim 1; claim 2; claim 3; claim 4; claim 5; claim 11; claim 22; claim 24; claim 30; claim 34; claim 38; claim 40; claim 42; claim 44; claim 46; claim 48; claim 50; claim 52; Specification: figs. 1, 2, 5, 9, 11; col. 2:38-39; col. 2:41-50; col. 2:55-3:11; col. 3:15-22; col. 3:25-28; col. 3:33-38; col. 3:44-51; col. 3:61-65; col. 3:67-4:11; col. 4:21-23; col. 4:50-51; col. 5:50-54; col. 5:56-58; col. 6:9-13; col. 6:15-19; col. 6:23-25; col. 6:27-44; col. 6:48-59; col. 7:41-43; col. 9:4-6; col. 10:30-33; col. 10:42-45; col. 12:58-61; col. 12:30-37; col. 12:39-43; col. 12:50-58; col. 12:60-65; col. 13:12-14; col. 14:1-4; col. 18:4-18; col. 18:27-30; col. 18:35-40; col. 18:47-51; col. 18:62-19:9; col. 19:14-17; col. 19:19-23; col. 19:42-47; col. 19:55-59; col. 24:17-25; col. 24:34-36; col. 24:38-40; col. 24:48-59; col. 24:62-68; col. 25:11-24; col. 25:41-47; col. 25:53-68; col. 26:1-18; col. 26:29-34; col. 29:33-39; col. 29:59-67; col. 30:10-13; col. 30:15-41; col. 30:49-52; col. 30:56-58; col. 31:25-28; col. 31:31-40; col. 31:50-52; col. 32:2-4; col. 32:15-22; col. 32:50-55; col. 33:59-62; col. 33:64-67; col. 34:25-32; col. 37:23-26; col. 37:42-46; col. 38:12-22; col. 39:55-57; col. 41:51-55; col. 41:65; col. 41:67-42:2; col. 42:5-16; see also Prosecution History: Notice of Allowability, Oct. 14, 1993, pp. 2-3. EXTRINSIC EVIDENCE:		Newton's Telecom Dictionary: "**Logic**…a system that could be applied to the relationships between propositions to which only a binary choice of truth existed, i.e., yes or no." IBM Dictionary of Computing (10th ed. 1993): The systematized interconnection of digital switching functions, circuits, or devices. EXPERT TESTIMONY: Realtek's expert, Dr. Izhak Rubin, may provide testimony as to the definition of the disputed terms as would be understood by one of ordinary skill in the relevant art and may provide an explanation of the technology.

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	3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action. See also U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and 6,570,884; Joint Claim Construction Statement in Cv-05-00098 (VRW). 3Com reserves the right to rely on any statement made by any party under the Patent Local Rules.		
"**threshold value**" found in claim numbers: '459 patent: 1 also presented for construction in: '872 patent: 10 '094 patent: 47	PROPOSED CONSTRUCTION: A value representing the quantity of data sufficient to trigger the initiation of some process DICTIONARY/TREATISE DEFINITIONS: threshold: The American Heritage Dictionary of the English Language (4th ed. 2000): The point that must be exceeded to begin producing a given effect or result or to elicit a response; see also Dictionary of Computing (1st ed. 1983): Threshold element: A logic element whose output is determined by comparing a weighted sum of inputs with a predetermined/prescribed threshold value. If the threshold is exceeded, the output is a logic 1; if not, the output is logic 0. If the number of inputs is odd, if the weights are all equal,	PROPOSED CONSTRUCTION: A set value indicating a desired limit. REFERENCES: PATENT SPECIFICATION: "If host processor 5 responds to network adapter 3 before a complete data frame is transferred, host processor 5 then may decrease the *threshold value* in alterable storage location 10a enabling threshold logic 10 to generate the indication signal at a later time in the next transfer of a data frame. Alternatively, if host processor 5 responds to the network adapter 3 after a complete data frame has already been transferred, host processor 5 may then increase the threshold value in alterable storage location 10a enabling the threshold logic to generate an	PROPOSED CONSTRUCTION: A number corresponding to a level of data required for some process to take place. DICTIONARY/TREATISE DEFINITIONS: threshold The American Heritage Dictionary of the English Language (4th ed. 2000): The point that must be exceeded to begin producing a given effect or result or to elicit a response. McGraw-Hill Electronics Dictionary (fifth edition, 1994) Threshold: 1. The least value of a current, voltage, or other quantity that produces the minimum detectable response. It is also called a limen. 2. The level of pumping at which a laser can go into self-excited

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	and the threshold is equal to half of the number of inputs, then the threshold element behaves as a majority element. A system of threshold elements is described by or as threshold logic. INTRINSIC EVIDENCE: Claims: claim 1; claim 5; claim 8; claim 9; claim 10; claim 15; claim 16; claim 18; claim 20; claim 22; claim 23; claim 27; claim 28; claim 29; claim 33; claim 34; claim 35; claim 36; claim 37; claim 40; claim 41; claim 44; claim 45; claim 50; claim 51; claim 52; claim 53; Specification: see, e.g., fig. 2; col. 3:67-4:2 ("The transfer threshold logic includes an alterable storage location containing a transfer threshold value representing an amount of the data frame to be transferred before generating a transfer complete indication"); see also col. 2:46-50; col. 2:52-54; col. 3:11-14; col. 3:18-25; col. 3:28-32; col. 3:37-46; col. 3:51-57; col. 4:7-11; col. 4:50-51; col. 6:32-40; col. 6:48-59; col. 21:40-42; col. 30:15-25; col. 30:45-48; col. 30:49-52; col. 31:19-22; col. 32:6-8; col. 32:13-15; col. 32:37-39; col. 35:39-41; col. 35:43-45; col. 35:52-56; col. 36:45-47; col. 39:66-67; col. 40:26-32; col. 41:51-55; col. 41:67-42:4; col. 42:19-22; Col. 42: 17-25; Col. 1: 46-51; Col. 1: 63-66; Col. 2: 46-54; Col. 2: 30-35; Col. 2: 23-27; Col. 41: 44-55; 459; Col. 6: 9-59; Col. 3: 11-14; see also Prosecution History: Notice of	indication signal at an earlier time in the next transfer of a data frame." ('459; Col. 6: 48-59) (emphasis added). "The above indication signals are further optimized by allowing the host processor to *dynamically tune* the timing of the indication signals. The host processor has write access to the threshold registers and may alter the *threshold values* in the threshold registers based on posted status information by the network adapter. The posted status information will allow the host processor to determine whether it is responding too early or too late to an interrupt generated by the indications." ('459; Col. 42: 17-25) (emphasis added). "The control means also posts status information which may be used by the host processor as feedback for optimizing the *threshold value* in the *alterable storage location*." ('459; Col. 3: 11-14) (emphasis added). "Threshold logic 10 in network adapter 3 is designed for eliminating or reducing interrupt latency. Threshold logic 10 makes a determination of how much of a data frame is transferred before generating an early indication signal. The early indication signal may then cause an early interrupt signal to be generated during the transfer of a data frame. Moreover, threshold	oscillation. threshold value McGraw-Hill Electronics Dictionary (fifth edition, 1994) Threshold Value: The minimum input that produces a corrective action in an automatic control system. EXPERT TESTIMONY: Realtek's expert, Dr. Izhak Rubin, may provide testimony as to the definition of the disputed terms as would be understood by one of ordinary skill in the relevant art and may provide an explanation of the technology.

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	Allowability, Oct. 14, 1993, pp. 2-3. EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action. See also U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and 6,570,884; Joint Claim Construction Statement in Cv-05-00098 (VRW). 3Com reserves the right to rely on any statement made by any party under the Patent Local Rules.	logic 10 is designed such that the time required for transferring the remainder of the data frame should approximately equal the time required for host processor 5 save its system parameters. Therefore, interrupt latency is eliminated or reduced by allowing host processor 5's interrupt routine to coincide with the transfer of the remainder of the data frame. FIG. 2 is a functional block diagram of network adapter 3 with threshold logic 10 illustrating the various transfer paths. Network adapter 3 contains transceiver 12 which transmits and receives data frames across network 2. Network interface logic 11 is responsible for the transfer of a data frame between network buffer 9 and transceiver 12. Likewise, the network adapter 3 contains host interface logic 8 which is responsible for transferring a data frame between network buffer 9 and host system 1. Threshold logic 10 contains an alterable storage location 10a which contains a *threshold value*. This *threshold value* represents the amount of a data frame which will be transferred into or out of buffer 9 before an early indication signal will be generated which may cause host interface logic 8 to send an interrupt to host processor 5. Host processor 5 has access to the alterable storage 10a location containing the *threshold value* through host interface logic 8. The threshold logic	

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		also includes a means for the host processor 5 to dynamically alter the time at which an indication is generated based on prior host processor 5 responses. When responding to an interrupt generated by an early indication, the host processor may examine network adapter status information to determine if host processor 5 is servicing the interrupt too early or too late. If host processor 5 responds to network adapter 3 before a complete data frame is transferred, host processor 5 then may decrease the threshold value in alterable storage location 10a enabling threshold logic 10 to generate the indication signal at a later time in the next transfer of a data frame. Alternatively, if host processor 5 responds to the network adapter 3 after a complete data frame has already been transferred, host processor 5 may then increase the threshold value in *alterable storage location* 10a enabling the threshold logic to generate an indication signal at an earlier time in the next transfer of a data frame." ('459; Col. 6: 9-59) (emphasis added). "Therefore, the present invention reduces host processor interrupt latency by generating early indications of data frame transfers. These early indications then may be used to generate an early interrupt to the host processor before the data frame is transferred which allows the host processor to	

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		save its current environment during a data frame transfer. The early indications are generated by threshold logic which determines how much of a data frame is transferred before generating an early indication by comparing a *threshold value* in a threshold register to a data transfer counter." ('459; Col. 41: 44-55) (emphasis added). "Therefore, it is desirable to provide a network adapter with an optimized indication signal to the host processor of the completion of the transfer of a data frame which reduces interrupt latency allowing for optimized network adapter/host system performance." ('459; Col. 2: 23-27). "The present invention provides for optimized indication signals to a host processor by a network adapter of the completion of a transfer of a data frame. The apparatus is coupled between a network transceiver and a host system which includes a host processor and host memory." ('459; Col. 2: 30-35). "The threshold logic includes a counter coupled to the buffer memory for counting the data transfer to or from the buffer memory, and an alterable storage location containing a *threshold value*. Means for comparing the counter and the alterable storage location is also provided.	

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		The indication signal to the host is generated based on the comparison of the counter and the *threshold value* in the alterable storage location." ('459; Col. 2: 46-54) (emphasis added). "As can be seen, there is interrupt latency between when the network adapter has completed a transfer and when the host processor is able to service the interrupt generated by the network adapter." ('459; Col. 1: 63-66). "In prior art systems, such as the National Semiconductor DP83932B, a systems-oriented network interface controller (SONIC) and the Intel 82586 local area network co-processor, an interrupt is generated by the network adapter to the host processor on the completion of a data transfer." ('459; Col. 1: 46-51). EXTRINSIC EVIDENCE: *EXPERT TESTIMONY:* D-Link's expert, Howard Frazier, may provide testimony as to the definition of the disputed terms as would be understood by one of ordinary skill in the relevant art and may provide an explanation of the technology. *DICTIONARY/TREATISE DEFINITIONS:* Webster's Ninth New Collegiate Dictionary (1983), pg.229:	

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		Threshold - "A level, point, or value above which something is true or will take place and below which it is not or will not." D-Link also incorporates by reference Realtek's references.	

2. U.S. Pat. No. 5,434,872

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
"**falls behind**" found in claim numbers: '872 patent: 1	PROPOSED CONSTRUCTION: underruns DICTIONARY/TREATISE DEFINITIONS: See "**a condition in which the means for transferring falls behind the transmit logic**" for definitions of "falls behind." INTRINSIC EVIDENCE: Claims: see, e.g., claim 15 ("an underrun condition in which the host interface means in transferring data to the buffer memory falls behind the network interface means in transferring data to the transceiver"); claim 25 ("a condition in which the data transfer circuitry falls behind the medium access controller"); see also claim 1; claim 18; Specification: fig. 18; col. 28:48-29:2 ("According to the present invention, this transmit data path includes an underrun detector 413 for detecting a condition in which the transferring of data into the transmit data buffer, or immediate data to the transmit descriptor buffer,	PROPOSED CONSTRUCTION: The absence of a write signal during a specified interval. INTRINSIC EVIDENCE: PATENT SPECIFICATION: "[U]nderrun detector 413 for detecting a condition in which the transferring of data into the transmit data buffer, or immediate data to the transmit descriptor buffer, by the host interface falls behind the transferring of data into the transmit data path 400 by the transmit DMA logic. The underrun detector 413 is controlled by the transmit control logic 411. The transmit control logic 411 indicates intervals across line 414 during which a transmit write TXWR signal is expected on line 402. The underrun detector determines that a transmit write TXWR signal is not present during an expected interval of the frame transmission, then a bad frame signal is generated on line 409."	PROPOSED CONSTRUCTION: A condition in which the transferring of data by the host interface falls behind the transferring of data by a transmit logic. INTRINSIC EVIDENCE: '872 patent at 28:48-29:2 ("According to the present invention, this transmit data path includes *an underrun detector 413* for detecting *a condition in which the transferring of data into the transmit data buffer*, or immediate data to the transmit descriptor buffer, *by the host interface falls behind the transferring of data into the transmit data path 400 by the transmit DMA logic*. . . . The underrun detector determines that a transmit write TXWR signal is not present during an expected interval of the frame transmission, then a bad frame signal is generated on line 409. . . .") EXPERT TESTIMONY:

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	by the host interface falls behind the transferring of data into the transmit data path 400 by the transmit DMA logic. The underrun detector 413 is controlled by the transmit control logic 411. The transmit control logic 411 indicates intervals across line 414 on line 402. The underrun detector determines that a transmit write TXWR signal in not present during an expected interval of the frame transmission, then a bad frame signal is generated on line 409. In response to the bad frame signal, the CRC data is inverted by the exclusive OR gate 407 which causes a bad CRC to be generated for the already transmitted portions of the frame suffering the underrun. Transmit control logic 411 also responds to the bad frame signal on line 409 to select the bad CRC data through multiplexer 410. Finally, the bad frame signal on line 409 in used for posting status information through the xmitFailureRegister of an underrun condition."); Col. 28:48-29:2; see also Prosecution History: Office Action, Oct. 26, 1993, p. 3; Response to Office Action, Oct. 5, 1994, p. 2. EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term.	('872; Col. 28: 49-61). PROSECUTION HISTORY: In the '872 prosecution history in an Amendment mailed October 5, 1994, Applicants amended claim 1 to overcome a prior art reference. Applicants added, *inter alia*, the following phrase to claim 1: "means for transferring falls behind the transmit logic . . ." (See '872 Prosecution History, Amendment mailed October 5, 1994, p. 3). EXTRINSIC EVIDENCE: *EXPERT TESTIMONY:* D-Link's expert, Howard Frazier, may provide testimony as to the definition of the disputed terms as would be understood by one of ordinary skill in the relevant art and may provide an explanation of the technology.	Realtek's expert, Dr. Izhak Rubin, may provide testimony as to the definition of the disputed terms as would be understood by one of ordinary skill in the relevant art and may provide an explanation of the technology.

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	3Com reserves the right to rely on testimony by any expert in this action. See also U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and 6,570,884, (in particular, dependent claims 4 and 6 of the '094); Joint Claim Construction Statement in Cv-05-00098 (VRW). 3Com reserves the right to rely on any statement made by any party under the Patent Local Rules.		
"**a condition in which the means for transferring falls behind the transmit logic**" found in claim numbers: '872 patent: 1	PROPOSED CONSTRUCTION: A transmission underrun condition. DICTIONARY/TREATISE DEFINITIONS: See "**logic**" below; condition: The American Heritage Dictionary of the English Language (4th ed. 2000): A mode or state of being . . . . A state of readiness or physical fitness. One that is indispensable to the appearance or occurrence of another; prerequisite . . . ; transfer: The American Heritage Dictionary of the English Language (4th ed. 2000): The conveyance or removal of something from one place, person, or thing to another. One who transfers or is transferred, as to a new school. A design conveyed by contact from one surface to another. A ticket entitling a passenger to change from one public conveyance to another as part of one trip. A place where such a change is made. Law. A conveyance of title or property from one person to another. fall behind: The American	PROPOSED CONSTRUCTION: "Means for transferring" requires means-plus-function analysis; see 35 U.S.C. 112(6) analysis in Section B. See also "falls behind." If separately construed, D-Link would propose the construction proposed by Realtek.	PROPOSED CONSTRUCTION: A condition in which the transferring of data into a transmit data buffer by the host interface falls behind the transferring of data into a transmit data path by a transmit logic. INTRINSIC EVIDENCE: '872 patent at 28:48-29:2 ("According to the present invention, this transmit data path includes an underrun detector 413 for detecting a condition in which the transferring of data into the transmit data buffer, or immediate data to the transmit descriptor buffer, by the host interface falls behind the transferring of data into the transmit data path 400 by the transmit DMA logic. . . . The underrun detector determines that a transmit write TXWR signal is not present during an expected interval of the frame transmission, then a bad frame signal is generated on line 409. . . . ") EXPERT TESTIMONY:

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	Heritage Dictionary of the English Language (4th ed. 2000): To fail to keep up a pace; lag behind. transmit: The American Heritage Dictionary of the English Language (4th ed. 2000): To send from one person, thing, or place to another; convey. See Synonyms at convey. See Synonyms at send1. To cause to spread; pass on: transmit an infection. To impart or convey to others by heredity or inheritance; hand down. To pass along (news or information); communicate. Electronics. To send (a signal), as by wire or radio. Physics. To cause (a disturbance) to propagate through a medium. To convey (force or energy) from one part of a mechanism to another. To send out a signal. INTRINSIC EVIDENCE: Claims: see, e.g., claim 15 ("an underrun condition in which the host interface means in transferring data to the buffer memory falls behind the network interface means in transferring data to the transceiver"); claim 25 ("a condition in which the data transfer circuitry falls behind the medium access controller"); see also claim 1; claim 18; Specification: fig. 18; col. 28:48-29:2 ("According to the present invention, this transmit data path includes an underrun detector 413 for detecting a condition in which the transferring of data into the transmit data buffer, or immediate data to the transmit descriptor buffer, by the host interface falls behind the transferring of		Realtek's expert, Dr. Izhak Rubin, may provide testimony as to the definition of the disputed terms as would be understood by one of ordinary skill in the relevant art and may provide an explanation of the technology.

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	data into the transmit data path 400 by the transmit DMA logic. The underrun detector 413 is controlled by the transmit control logic 411. The transmit control logic 411 indicates intervals across line 414 on line 402. The underrun detector determines that a transmit write TXWR signal in not present during an expected interval of the frame transmission, then a bad frame signal is generated on line 409. In response to the bad frame signal, the CRC data is inverted by the exclusive OR gate 407 which causes a bad CRC to be generated for the already transmitted portions of the frame suffering the underrun. Transmit control logic 411 also responds to the bad frame signal on line 409 to select the bad CRC data through multiplexer 410. Finally, the bad frame signal on line 409 in used for posting status information through the xmitFailureRegister of an underrun condition."); see also Prosecution History: Office Action, Oct. 26, 1993, p. 3; Response to Office Action, Oct. 5, 1994, p. 2. EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any		

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	expert in this action. See also U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and 6,570,884 (in particular, dependent claims 4 and 6 of the '094); Joint Claim Construction Statement in Cv-05-00098 (VRW). 3Com reserves the right to rely on any statement made by any party under the Patent Local Rules.		
"**underrun**" found in claim numbers: '872 patent: 1 also presented for construction in: '094 patent: 21	PROPOSED CONSTRUCTION: When expected data from a frame to be transferred is not available DICTIONARY/TREATISE DEFINITIONS: IBM Dictionary of Computing (10th ed. 1993): Loss of data caused by inability of a transmitting device or channel to provide data to the communication control logic (SDLC or BSC/SS) at a rate that is fast enough for the attached data link or loop; see also The American Heritage Dictionary of the English Language (4th ed. 2000): Something that runs under, as: a. An amount or a quantity produced that is less than what has been estimated. b. The difference between this amount or quantity and what has been estimated. INTRINSIC EVIDENCE: Claims: see, e.g., claim 15 ("an underrun condition in which the host interface means in transferring data to the buffer memory falls behind the network interface means in transferring data to the transceiver"); claim 25 ("a condition in which the	PROPOSED CONSTRUCTION: The condition of falling behind. See proposed construction for "falls behind."	PROPOSED CONSTRUCTION: A condition in which the transferring of data into a transmit data buffer by the host interface falls behind the transferring of data into a transmit data path by a transmit logic. INTRINSIC EVIDENCE: '872 patent at 28:48-29:2 ("According to the present invention, this transmit data path includes *an underrun detector 413 for detecting a condition in which the transferring of data into the transmit data buffer, . . . , by the host interface falls behind the transferring of data into the transmit data path 400 by the transmit DMA logic*. . . . The underrun detector determines that a transmit write TXWR signal is not present during an expected interval of the frame transmission, then a bad frame signal is generated on line 409. . . . ") EXPERT TESTIMONY: Realtek's expert, Dr. Izhak Rubin, may provide testimony as to the

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	data transfer circuitry falls behind the medium access controller"); see also claim 1; claim 18; Specification: fig. 18; col. 28:48-29:2 ("According to the present invention, this transmit data path includes an underrun detector 413 for detecting a condition in which the transferring of data into the transmit data buffer, or immediate data to the transmit descriptor buffer, by the host interface falls behind the transferring of data into the transmit data path 400 by the transmit DMA logic. The underrun detector 413 is controlled by the transmit control logic 411. The transmit control logic 411 indicates intervals across line 414 on line 402. The underrun detector determines that a transmit write TXWR signal in not present during an expected interval of the frame transmission, then a bad frame signal is generated on line 409. In response to the bad frame signal, the CRC data is inverted by the exclusive OR gate 407 which causes a bad CRC to be generated for the already transmitted portions of the frame suffering the underrun. Transmit control logic 411 also responds to the bad frame signal on line 409 to select the bad CRC data through multiplexer 410. Finally, the bad frame signal on line 409 in used for posting status information through the xmitFailureRegister of an underrun condition."); see also Prosecution History: Office Action, Oct. 26, 1993, p. 3; Response to		definition of the disputed terms as would be understood by one of ordinary skill in the relevant art and may provide an explanation of the technology.

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	Office Action, Oct. 5, 1994, p. 2. EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action. See also U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and 6,570,884 (in particular, dependent claims 4 and 6 of the '094); Joint Claim Construction Statement in Cv-05-00098 (VRW). 3Com reserves the right to rely on any statement made by any party under the Patent Local Rules.		
"**underrun control logic**" found in claim numbers: '872 patent: 1	PROPOSED CONSTRUCTION: Logic that detects underruns. DICTIONARY/TREATISE DEFINITIONS: See "**underrun**" in this subsection and "**logic**" in subsection 1. INTRINSIC EVIDENCE: Claims: see, e.g., claim 15 ("an underrun condition in which the host interface means in transferring data to the buffer memory falls behind the network interface means in transferring data to the transceiver"); claim 25 ("a condition in which the data transfer circuitry falls behind the medium access	See proposed construction pursuant to 35 U.S.C. § 112 ¶ 6 in Section B.	Please refer to the construction under 35 U.S.C. § 112 ¶ 6. To the extent this term requires construction, Realtek asserts that "logic" should be construed as "means" and, therefore, this claim element should be governed by 35 U.S.C. § 112 ¶ 6. If the Court determines that 35 U.S.C. § 112 ¶ 6 does not apply, "underrun control logic" should be construed as "device for controlling underrun." DICTIONARY/TREATISE DEFINITIONS: Synopsis, Inc., Electronic Design Automation Glossary of Terms

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	controller, and supplies a bad frame signal to the network"); see also claim 1; claim 26; Specification: see, e.g., fig. 18; col. 28:25-27; see also Prosecution History: Office Action, Oct. 26, 1993, p. 3; Response to Office Action, Oct. 5, 1994, p. 2. EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action. See also U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and 6,570,884 (in particular, dependent claims 4 and 6 of the '094); Joint Claim Construction Statement in Cv-05-00098 (VRW). 3Com reserves the right to rely on any statement made by any party under the Patent Local Rules.		The sequence of functions performed by hardware or software. Hardware logic is made up of circuits that perform an operation. Software logic is the sequence of instructions in a program. Newton's Telecom Dictionary: "**Logic**…a system that could be applied to the relationships between propositions to which only a binary choice of truth existed, i.e., yes or no." IBM Dictionary of Computing (10th ed. 1993): The systematized interconnection of digital switching functions, circuits, or devices. EXPERT TESTIMONY: Realtek's expert, Dr. Izhak Rubin, may provide testimony as to the definition of the disputed terms as would be understood by one of ordinary skill in the relevant art and may provide an explanation of the technology.
"**bad frame signal**" found in claim numbers: '872 patent: 1 also presented for construction in: '094 patent: 21	PROPOSED CONSTRUCTION: A signal that a frame is bad. DICTIONARY/TREATISE DEFINITIONS: See "**frame(s)**" in subsection 1 for definitions of that term and "**indication signal**" in subsection 1 for definitions of "signal." bad: The American Heritage Dictionary of the English Language (4th ed. 2000): adj. 1. Not achieving an	PROPOSED CONSTRUCTION: A specific signal flag indicating that a corresponding frame contains invalid data.	PROPOSED CONSTRUCTION:: a signal indicating that a frame is bad. DICTIONARY/TREATISE DEFINITIONS: signal Newton's' Telecom Dictionary (fourth edition, 1991) Signal: 1. An electrical wave used to convey information 2. An alert. 3.

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	adequate standard; poor: a bad concert. . . . 8. Injurious in effect; detrimental: bad habits. 9. Not working properly; defective: a bad telephone connection. 10. Full of or exhibiting faults or errors: bad grammar. INTRINSIC EVIDENCE: Claims: see, e.g., claim 4 ("the bad frame signal comprises a corrupted error detection code"); see also claim 1; claim 15; claim 16; claim 18; claim 20; claim 25; claim 26; Specification: see, e.g., fig. 18; col. 19:35-38; col. 28:38-40; col. 28:48-29:2; Fig. 18; col. 28:58-29:2; 29:40-44; see also Prosecution History: Office Action, Oct. 26, 1993, p. 3; Office Action, Oct. 26, 1993, p. 6; Response to Office Action, Oct. 5, 1994, p. 2; Response to Office Action, Oct. 5, 1994, p. 3. EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action. See also U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and 6,570,884; Joint Claim Construction Statement in Cv-05-00098 (VRW). 3Com reserves the right to		An acoustic device (e.g. a bell) or a visual device (e.g. a lamp) which calls attention. To transmit an information signal or alerting signal. McGraw Hill Electronics Dictionary (fifth edition, 1994) Signal: Any variation in an electrical current, visible or nonvisible light, audible or ultrasonic energy that conveys information. Signals can be coded in frequency, phase, or amplitude to separate them from unwanted noise. bad: The American Heritage Dictionary of the English Language (4th Ed. 2000): adj. 1. Not achieving an adequate standard; poor: a bad concert. . . . 8. Injurious in effect; detrimental: bad habits. 9. Not working properly; defective: a bad telephone connection. 10. Full of or exhibiting faults or errors: bad grammar. INTRINSIC EVIDENCE: '872 patent at 28:48-29:2; '094 patent at 27: 15-35 ("According to the present invention, this transmit data path includes *an underrun detector 413* for detecting *a condition in which the transferring of data into the transmit data buffer, . . ., by the host interface falls behind the transferring of data into the transmit data path 400 by the transmit DMA logic*. . . . The underrun detector

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	rely on any statement made by any party under the Patent Local Rules.		determines that a transmit write TXWR signal is not present during an expected interval of the frame transmission, *then a bad frame signal is generated on line 409*. . . .") '872 patent, Fig. 18; '094 patent, Fig. 18 ("a signal line identified as "bad frame" and connected "to host interface.") EXPERT TESTIMONY: Realtek's expert, Dr. Izhak Rubin, may provide testimony as to the definition of the disputed terms as would be understood by one of ordinary skill in the relevant art and may provide an explanation of the technology.
"**buffer**" found in claim numbers: '872 patent: 1, 10, 21 also presented for construction in: '459 patent: 1 '094 patent: 1, 9, 21, 28, 39, 47	PROPOSED CONSTRUCTION: A memory for temporary storage of data. DICTIONARY/TREATISE DEFINITIONS: See "**buffer**" in subsection 1. INTRINSIC EVIDENCE: Claims: see, e.g., claim 2 ("the transmit buffer includes a transmit descriptor ring and a *transmit data buffer*"); claim 7 ("The apparatus of claim 1, wherein the buffer includes a transmit descriptor ring buffer and a transmit data buffer, and the means for transferring includes: transmit descriptor logic for mapping transmit descriptors from the system to the transmit descriptor ring buffer; and download logic, responsive to the transmit descriptors in the transmit descriptor ring	PROPOSED CONSTRUCTION: Term is used only in phrase "buffer memory." See construction of "buffer memory."	Same as "**buffer memory**" identified above.

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	buffer, for retrieving data from memory in the system and storing retrieved data in the transmit data buffer."); see also claim 1; claim 3; claim 9; claim 10; claim 11; claim 15; claim 18; claim 21; claim 22; Specification: see, e.g., figs. 2, 6-10E; col 1:47-54 ("Transmit data buffers are to be distinguished from first-in-first-out FIFO systems, in which the sending system downloads data of a frame into the FIFO, while the network adapter unloads the FIFO during a transmission. The data in FIFOs cannot be retained and reused by the media access control functions, or by the host, like data in transmit data buffers."); col. 1:65-67 ("Furthermore, the prior art systems which use transmit data buffers require the host or sending system to manage the transmit data buffer."); col. 2:13-18 ("The present invention provides for the early initiation of transmission of data in a network interface that includes a dedicated transmit buffer."); col. 2:35-37 ("the transmit data buffer includes a transmit descriptor ring, and a transmit data buffer"); col. 13:12-27 ("In the preferred system, the adapter uses 32K bytes of static RAM for the transmit buffers, receive buffers, control structures, and various status and statistics registers. Several of the regions in the adapter's memory defined in Fig. 5 provide defined data structures. A. Transmit Data Buffer The transmit data buffer occupies 3K		

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	bytes as mentioned above. This region is divided into two 1.5K buffers. Only the data that are downloaded to the adapter via bus master transfers are stored in these buffers. The controller will use both the contents of the transmit data buffer and the immediate data portion of the transmit descriptors, when encapsulating a frame for transmission. The adapter automatically alternates the use of the buffers after choosing the buffer closest to the base of the memory as the power up default."); see also col. 1:36-2:10; col. 2:14-27; col. 2:44-48; col. 3:21-27; col. 3:59-65; col. 4:29-33; col. 4:38-45; col. 4:64-5:22; col. 5:41-43; col. 5:57-61; col. 6:33-35; col. 8:57-64; col. 9:1-3; col. 9:8-11; col. 9:13-16; col. 9:19-22; col. 9:29-32; col. 9:37-39; col. 9:62-65; col. 9:68-10:7; col. 10:16-18; col. 10:20-23; col. 11:17-20; col. 11:22-25; col. 11:33-39; col. 11:59-61; col. 12:4-6; col. 12:43-46; col. 12:58-68; col. 13:2-8; col. 13:12-15; col. 13:17-48; col. 13:52-54; col. 13:61-66; col. 14:17-20; col. 15:25-46; col. 15:58-60; col. 16:1-7; col. 16:9-12; col. 16:28-32; col. 16:35-39; col. 16:52-56; col. 16:67-17:3; col. 17:7-22; col. 17:24-31; col. 17:33-34; col. 17:54-56; col. 17:65-68; col. 18:21-25; col. 18:44-46; col. 18:49-52; col. 19:45-47; col. 21:22-26; col. 21:42-45; col. 22:60-62; col. 22:1-2; col. 22:4-8; col. 22:20-23; col. 22:27-32; col. 22:44-51; col. 22:53-56; col. 22:67-23:4; col. 23:43-45; col. 23:48-51; col. 23:60-65; col. 24:26-27; col. 24:29-32; col.		

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	24:37-39; col. 24:39-40; col. 24:43-52; col. 25:48-50; col. 28:48-54; col. 29:5-9; col. 29:25-31; see also Prosecution History: Office Action, Oct. 26, 1993, p. 2; Office Action, Oct. 26, 1993, p. 3; Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 5; Office Action, Oct. 26, 1993, p. 6; Part 131 Affidavit, p. 1; Part 131 Affidavit, p. 2; Part 131 Affidavit, p. 3; Part 131 Affidavit, p. Ex. 1, p. 6; Response to Office Action, Feb. 23, 1994, p. 2; Response to Office Action, Feb. 23, 1994, pp. 4-5; Response to Office Action, Feb. 23, 1994, p. 5; Response to Office Action, Feb. 23, 1994, p. 6; Office Action, Jul. 6, 1994, p. 2; Response to Office Action, Oct. 5, 1994, p. 2; Response to Office Action, Oct. 5, 1994, p. 3. EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action. See also section I.A, supra (agreed upon definition for "buffer" in '625 and '884 patents); U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and 6,570,884; Joint Claim Construction Statement in		

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	Cv-05-00098 (VRW). 3Com reserves the right to rely on any statement made by any party under the Patent Local Rules.		
"**buffer memory**" found in claim numbers: '872 patent: 1, 10, 21 also presented for construction in: '459 patent: 1 '094 patent: 1, 9, 21, 28, 39, 47	PROPOSED CONSTRUCTION: A memory for temporary storage of data. DICTIONARY/TREATISE DEFINITIONS: See "**buffer**" and "**memory**" in subsection 1. INTRINSIC EVIDENCE: Claims: see, e.g., claim 2 (depending from claims 1 and including a limitation that "the transmit buffer includes a transmit descriptor ring and a *transmit data buffer*"); see also claim 1; claim 3; claim7; claim 10; claim 11; claim 15; claim 18; claim 21; claim 22; Specification: see, e.g., col. 2:35-37 ("the transmit data buffer includes a transmit descriptor ring, and a transmit data buffer"); see also col. 1:14-16; col. 2:13-17; col. 1:36-2:6; col. 3:59-65; col. 5:57-61; col. 13:18-48; col. 13:59-68; see also Prosecution History: Office Action, Oct. 26, 1993, p. 2; Office Action, Oct. 26, 1993, p. 2; Office Action, Oct. 26, 1993, p. 3; Part 131 Affidavit, p. 1; Part 131 Affidavit, p. 2; Response to Office Action, Feb. 23, 1994, p. 2; Response to Office Action, Oct. 5, 1994, p. 2. EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael	PROPOSED CONSTRUCTION: Dedicated random access memory that (1) stores transmit data, (2) is distinct from a FIFO, (3) can always retransmit a frame of data without having to retrieve it from a host, and (4) is controlled independently of the host system. REFERENCES: PATENT SPECIFICATION: Claim 2 of the '872 patent recites "The apparatus of claim 1, wherein the *transmit buffer* includes . . ." (emphasis added). Claim 7 of the '872 patent recites "The apparatus of claim 1, wherein the *buffer* includes a transmit descriptor ring buffer and a transmit data buffer . . ." (emphasis added). "Early initiation of transmission of data in a network interface that includes a dedicated *transmit buffer* is provided in a system which includes logic for transferring frames of data composed by the host computer into the transmit buffer." ('872 Abstract and '094 Abstract)[2] (emphasis added). "The present invention	Same as "**buffer memory**" identified above.

[2] Citations to the description of the '872 patent can also be found in the description of the related '094 patent; all citations to the '872 patent apply equally to the '094 patent.

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action. See also section I.A, supra (agreed upon definition for "buffer" in '625 and '884 patents); U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and 6,570,884; Joint Claim Construction Statement in Cv-05-00098 (VRW).	provides for the early initiation of transmission of data in a network interface that includes a *dedicated transmit buffer*. The system includes logic for transferring frames of data composed by the host computer into the transmit buffer." ('872; Col. 2: 13-17) (*See also* '872; Col. 1: 14-16) (emphasis added). "According to another aspect of the present invention, the *transmit buffer* includes a transmit descriptor ring, and a transmit data buffer. The host system composes a frame by storing a transmit descriptor in the adapter managed transmit descriptor ring." ('872; Col. 2: 35-39) (emphasis added). "Some network adapter interfaces include dedicated *transmit buffers* into which a frame of data composed by the sending system can be downloaded by the sending system. The frame is then stored in the *transmit data buffer* until the media access control functions associated with transmitting the frame on the network have successfully transmitted the frame, or cancelled the frame transmission. If the frame transmission is cancelled, the data may be retained in the *transmit data buffer* until the sending system initiates a second attempt to transmit the frame. Transmit data buffers are to be distinguished from first-in-first-out FIFO systems, in which the sending system downloads data of a frame	

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		into the FIFO, while the network adapter unloads the FIFO during a transmission. The data in FIFOs cannot be retained and reused by the media access control functions, or by the host, like data in *transmit data buffers*." ('872; Col. 1: 36-54) (emphasis added). "Although *transmit data buffers* enable a sending system to compose and download a frame into the *transmit data buffer*, and then attend to other tasks while the network adapter attempts to transmit the frame, it suffers the disadvantage that transmission of a frame is delayed until the entire frame has been downloaded into the buffer. Thus, *transmit data buffer* type systems improve host system efficiency at the expense of network throughput." ('872; Col. 1: 55-63) (emphasis added). "Furthermore, the prior art systems which use *transmit data buffers* require the host or sending system to manage the transmit data buffer. A network interface controller transfers data from the host managed transmit data buffer using DMA techniques through a FIFO buffer in the interface controller and on to the network." ('872; Col. 1: 65 - Col. 2: 2) (emphasis added). "Representative prior art systems include the National Semiconductor DP83932B, a systems-oriented network interface	

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		controller (SONIC) and the Intel 82586 local area network coprocessor." ('872; Col. 2: 3-6). "The *transmit data buffer* occupies 3K bytes as mentioned above. This region is divided into two 1.5K buffers. Only the data that are downloaded to the adapter via bus master transfers are stored in these buffers. The controller will use both the contents of the *transmit data buffer* and the immediate data portion of the transmit descriptors, when encapsulating a frame for transmission. The adapter automatically alternates the use of the *buffers* after choosing the *buffer* closest to the base of the memory as the power up default." ('872; Col. 13: 18-27) (emphasis added). "The *transmit buffers* are shared by the download DMA logic and the transmit DMA logic. The transmit DMA logic may switch from buffer 0 to buffer 1 and back again freely. The only restriction being the availability of transmit data as defined by the transmit start threshold register. The transmit DMA module switches from one buffer to the other whenever it has completed a transmission. The buffer switch occurs regardless of whether or not the transmission was successful and regardless of whether or not bus master download data were used in the preceding transmission." ('872; Col. 13: 28-38) (emphasis added).	

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		"The download DMA module may only switch from one *buffer* to the other, if the *buffer* it is going to switch to is not being used by the transmit DMA module. Download DMA will attempt to switch from one *buffer* to another every time it completes processing of a transmit descriptor as described below, regardless of whether or not any bus master operations were called for in the preceding descriptor. However, it will not change to a *buffer* that is in use by the transmit DMA module." ('872; Col. 13: 39-48) (emphasis added). "The *transmit data buffer* occupies 3K bytes as mentioned above. This region is divided into two 1.5K buffers. Only the data that are downloaded to the adapter via bus master transfers are stored in these buffers. The controller will use both the contents of the transmit data buffer and the immediate data portion of the transmit descriptors, when encapsulating a frame for transmission. The adapter automatically alternates the use of the buffers after choosing the buffer closest to the base of the memory as the power up default." ('459; Col. 13: 59-68) (emphasis added). PROSECUTION HISTORY: The following citation to the prosecution history of the '872 patent supports D-Link's proposed claim construction During prosecution of the	

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		application that issued as the '872 patent, in a Response dated February 23, 1994, 3Com stated the following: "Accordingly, the Firoozmand, et al. reference does not initiate transmission to the network upon the threshold determination. Rather, transmission to the network is initiated only when there is a full frame available in the buffer. When the token has been received by the transmitting station, and it has a full frame for transmission, then a transmission process is begun. The transmission process continues, relying on the threshold determination to keep the pipeline full, only while the token is held by the transmitting station." "The environment is substantially different from the CSMA/CD network, which begins transmission to the medium access controller as soon as the threshold determination is met for an incoming frame. The MAC may succeed in transmitting the frame, may suffer collisions, or may suffer other types of errors which require backoff. Thus, the adapter as claimed in new claims 24-29, initiates transmission without being assured that the medium access controller is able to gain access to the communications medium. *This is a much more sophisticated control environment than that required by the FDDI system of Firoozmand, et*	

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		al." Response dated February 23, 1994, p. 5. EXTRINSIC EVIDENCE: *PRIOR ART:* Datesheet for "82596CA High-Performance 32-Bit Local Area Network Coprocessor," November 1989, Intel Corp (Disclosed in D-Link's Preliminary Infringement Contentions), pg. 2: "Two large, independent FIFOs-128 bytes for Receive and 64 bytes for Transmit-tolerate long bus latencies and provide programmable thresholds that allow the user to optimize bus overhead for any worst-case bus latency." Datasheet for "The SUPERNET 2 Family for FDDI", October 1991, Advanced Micro Devices, Inc. (Disclosed in D-Link's Preliminary Infringement Contentions), pg. 2-37 : "The transmit FIFO (Figure 1) is a 36-bit by 9-word first-in-first-out register that temporarily stores data to be transmitted. In this way, continuity of data transmission is assured by providing a way to store a portion of the output data stream to compensate for delays involved in accessing the buffer memory." 1992 Local Area Network Databook Including Datasheet For DP83932B Systems-Oriented Network Interface Controller (SONIC), 1992, National Semiconductor Corp, pg.1-	

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		295: "The SONIC incorporates two independent 32-byte FIFOs for transferring data to/from the system interface and from/to the network. The FIFOs, providing temporary storage of data, free the host system from the real-time demands on the network." *DICTIONARY/TREATISE DEFINITIONS:* McGraw-Hill Illustrated Telecom Dictionary, Fourth Edition, 2001, pg. 83: Buffer - "A temporary storage (memory) device for data. A buffer is basically a box with RAM inside it. A common application for buffers is to collect a stream of data and temporarily store it until another device, such as a PC or server asks the buffer to download it. This is useful when the PC, server or LAN could be out of service for a period of time. When the server or PC is returned to service it just asks for the data from the buffer and it is downloaded. The buffer is then empty and ready to receive more data." *EXPERT TESTIMONY:* D-Link's expert, Howard Frazier, may provide testimony as to the definition of the disputed terms as would be understood by one of ordinary skill in the relevant art and may provide an explanation of the technology. D-Link also incorporates by reference Realtek's	

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		references.	
"**host system**" found in claim numbers: '872 patent: 1, 10, 21 also presented for construction in: '459 patent: 1 '094 patent: 1, 9, 21, 28, 39, 47 '884 patent: 1	PROPOSED CONSTRUCTION: A computer that communicates over a network DICTIONARY/TREATISE DEFINITIONS: Webster's New World Computer Dictionary (10th ed. 2003): 1. In the Internet, any computer that can function as the beginning and end point of data transfers. An Internet host has a unique Internet address (called an IP address) and a unique domain name. 2. In networks and telecommunications generally, a server that performs centralized functions, such as making program or data files available to other computers; The American Heritage Dictionary of the English Language (4th ed. 2000): Computer Science. A computer containing data or programs that another computer can access by means of a network or modem; Dictionary of Computing (3d ed. 1990): Host computer (host): A computer that is attached to a network and provides services other than simply acting as a store-and-forward processor or communication switch. INTRINSIC EVIDENCE: Claims claim 1; ; claim 10; ; claim 15; claim 18; ; claim 21; Specification: see, e.g., figs. 1-3; col.4:7-11 ("The network adapter 6 is, in turn, connected to an adapter memory 9, which is	PROPOSED CONSTRUCTION: Any system or computer that communicates over a network INTRINSIC EVIDENCE (872: Col 1: lns. 65-67) (094: Col. 1, lns. 60-62) Furthermore, the prior art systems which use transmit data buffers require the *host or sending system* to manage the transmit data buffer. (872: Col. 3, ln. 65 to col. 4., ln. 2) ('094: Col. 3, lns. 59-64) As shown in FIG. 1, such system for communicating data includes a host data processing system, generally referred to by reference number 1, which includes a host system bus 2, a host central processing unit 3, host memory 4, and other host devices 5, all communicating across the bus 2	PROPOSED CONSTRUCTION: Any system or computer that communicates over a network Evidence (872: Col 1: lns. 65-67) (094: Col. 1, lns. 60-62) Furthermore, the prior art systems which use transmit data buffers require the *host or sending system* to manage the transmit data buffer. (872: Col. 3, ln. 65 to col. 4., ln. 2) ('094: Col. 3, lns. 59-64) As shown in FIG. 1, such system for communicating data includes a host data processing system, generally referred to by reference number 1, which includes a host system bus 2, a host central processing unit 3, host memory 4, and other host devices 5, all communicating across the bus 2 (884: Col. 2, lns. 39-44) The invention is particularly suited to environments in which the host system is actively handling communications and other processing tasks, and in which the adapter is able to take over some specialized tasks without interfering with the active processing in the host system.

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	managed by the interface controller 6 or by the host CPU3"); see also col. 1; col. 1:51-55; col. 1:61-63; col. 1:65-67; col. 1-2:67-3; col. 2:16-18; col. 2:18-22; col. 2:27-31; col. 2:31-35; col. 2:37-39; col. 2:55-62; col. 3:44- 4:7; col. 3:11-14; col. 3:14-17; col. 3:17-19; col. 3: 59-4:2; col. 4:2-3; col. 4:11-13; col. 4:13-16; col. 4:19-21; col. 4:26-29; col. 4:29-30; col. 4:30-33; col. 4:33-34; col.4: 46-47; col.4: 47-50; col. 4:56-58; col. 4:58-61; col.4:61-62; col.4:62-64; col.4:64-67; col. 5:5-14; col. 5:14-20; col. 5:20-23; col. 5:28-31; col. 5:31-33; col. 5:33-36; col. 5:50-53; col. 5:57-60; col. 5:62-64; col.6:26-28; col.6:33-35; col.6:48-51; col.7:18-22; col.7:60-64; col.7:64-66; col. 8:5-7; col. 8:9-14; col. 8:28-29; col. 8:44-47; col. 8:55-57; col. 8:64-1; col. 9-10:68-4; col. 10:4-11; col. 10:14-16; col. 10:23-27; col. 10:27-31; col. 10:31-35; col. 10:35-38; col. 10:4-45; col. 10:60-63; col. 11:43-47; col. 11:47-49; col. 11:49-51; col. 11:51-53; col. 11:53-54; col. 11:54-57; col. 11:64-68; col. 11-12:68-4; col. 12:4-7; col. 12:15-17; col. 12:17-23; col. 12:23-24; col. 12:24-28; col. 12:33-37; col. 12:37-39; col. 12:39-41; col. 12:41-43; col. 12:49-50; col. 12:58-61; col. 12:61-65; col. 12:65-1; col. 13:1-2; col. 13:58-61; col. 13-14:67-4; col.14:4-6; col.14:30-33; col.14:36-38; col.14:49-53; col.14:56-58; col.14:62-65; col.14:65-68; col. 14-15:68-3; col.15:10-13; col.15:19-20; col.15:20-25; col.15:25-27; col.15:27-29; col.15:29-32; col.15:35-38; col.15:38-41; col.15:42-		

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	44; col.15:46-48; col.15:58-61; col.15:61-64; col.16:1-3; col.16:5-6; col.16:9-12; col.16:12-14; col.16:14-22; col.16:24-27; col.16:28-32; col.16:32-34; col.16:35-40; col.16:52-56; col.16:56-58; col.16:58-61; col.16:61-63; col.16:63-67; col. 16-17:67-3; col. 17:14-19; col. 17:33-38; col. 17:38-40; col. 17:40-46; col. 17:50-53; col. 17:56-59; col. 18:1-3; col. 18:6-10; col. 18:18-21; col. 18:21-25; col. 18:41-44; col. 18:47-49; col. 18:53-57; col. 19:3-5; col. 19:50-55; col. 20:14-17; col. 20:39-42; col. 20:63-66; col. 21:1-3; col. 21:7-11; col. 21:22-26; col. 21:49-51; col. 21:51-54; col. 22:63-66; col. 22:66-1; col. 22:1-4; col. 22:12-15; col. 22:15-16; col. 22:27-33; col. 22:33-34; col. 22:34-38; col. 22:38-39; col. 22:60-63; col. 22:63-65; col. 23:12-13; col. 24:47-52; col. 25:27-31; col. 25:48-51; col. 25:52-60; col. 26:9-10; col. 26:65-1; col. 27:33-35; col. 28:48-54; col. 29:39-40; col. 29:46-48; col. 29:48-51; see also Prosecution History: Office Action, Oct. 26, 1993, p. 2; Office Action, Oct. 26, 1993, p. 3; Office Action, Oct. 26, 1993, p. 5; Part 131 Affidavit, p. 2; Part 131 Affidavit, p. 2; Part 131 Affidavit, p. 2; Part 131 Affidavit, p. Ex. 1, p. 11; Part 131 Affidavit, p. Ex. 1, p. 11; Response to Office Action, Feb. 23, 1994, p. 2; Office Action, Jul. 6, 1994, p. 2; Office Action, Jul. 6, 1994, p. 2; Response to Office Action, Oct. 5, 1994, p. 2. EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael		

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action. See also U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and 6,570,884; Joint Claim Construction Statement in Cv-05-00098 (VRW). 3Com reserves the right to rely on any statement made by any party under the Patent Local Rules.		
"**logic**" found in claim numbers: '872 patent: 1, 21 also presented for construction in: '459 patent: 1 '625 patent: 23 '884 patent: 1	PROPOSED CONSTRUCTION: Circuitry and/or programming DICTIONARY/TREATISE DEFINITIONS: See "**logic**" in subsection 1. INTRINSIC EVIDENCE: Claims: claim 1; claim 4; claim 5; claim 7; claim 9; claim 11; claim 13; claim 14; claim 15; claim 19; claim 21; claim 22; claim 23; claim 25; claim 26; Specification: figs. 1, 2, 5, 9, 11-18; col. 2:16-18; col. 2:22-31; col. 2:48-51; col. 3:28-34; col. 3:37-44; col. 3:52-54; col. 4:11-16; col. 4:26-45; col. 4:47-49; col. 4:56-58; col. 4:67-5:13; col. 6:15-18; col. 7:44-46; col. 9:1-3; col. 9:13-16; col. 10:65-11:2; col. 11:25-31; col. 11:36-39; col. 11:51-61; col. 11:64-68; col. 12:7-15; col. 12:17-22; col. 12:37-39; col. 13:28; col. 13:29-31;	PROPOSED CONSTRUCTION: When used as a standalone term in the claims, "logic" is an unspecified claim element defined only by its function and thus requires interpretation under invokes 35 U.S.C. § 112 ¶ 6. In computer software or hardware context, "means" or "means for." See discussion in section below concerning 35 U.S.C. § 112 ¶ 6 constructions for phrases including "logic."	Please refer to the construction under 35 U.S.C. § 112 ¶ 6 for the separate claim limitations of the identified claims. To the extent this term requires construction, Realtek asserts that "logic" (or "logic for") as used in the identified claims should be construed as "means" (or "means for") and, therefore, the associated claim elements should be governed by 35 U.S.C. § 112 ¶ 6. If the Court determines that 35 U.S.C. § 112 ¶ 6 does not apply, "logic" should be construed as "device." DICTIONARY/TREATISE DEFINITIONS: Synopsis, Inc., Electronic Design Automation Glossary of Terms The sequence of functions performed by hardware or software. Hardware logic is

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	col. 16:9-23; col. 16:32-35; col. 16:40-45; col. 16:52-56; col. 16:67-17:14; col. 17:19-28; col. 17:47-50; col. 17:60-62; col. 21:49-50; col. 22:66-68; col. 22:1-4; col. 22:12-23; col. 22:26-32; col. 22:43-44; col. 22:48-59; col. 23:5-10; col. 23:20-29; col. 24:9-12; col. 24:17-18; col. 24:24-25; col. 24:32-34; col. 24:39-40; col. 24:48-52; col. 24:55-60; col. 24:67-25:2; col. 25:3-7; col. 25:19-21; col. 26:37-39; col. 26:46-49; col. 26:61-62; col. 27:36-38; col. 28:25-29; col. 28:33-45; col. 28:48-58; col. 28:65-67; see also Prosecution History: Office Action, Oct. 26, 1993, p. 2; Office Action, Oct. 26, 1993, p. 3; Part 131 Affidavit, pp. 2-3; Response to Office Action, Feb. 23, 1994, p. 5; Response to Office Action, Oct. 5, 1994, p. 2; Response to Office Action, Oct. 5, 1994, p. 3. EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action. See also U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and 6,570,884; Joint Claim Construction Statement in Cv-05-00098 (VRW). 3Com reserves the right to		made up of circuits that perform an operation. Software logic is the sequence of instructions in a program. Newton's Telecom Dictionary: "**Logic**…a system that could be applied to the relationships between propositions to which only a binary choice of truth existed, i.e., yes or no." IBM Dictionary of Computing (10th ed. 1993): The systematized interconnection of digital switching functions, circuits, or devices. EXPERT TESTIMONY: Realtek's expert, Dr. Izhak Rubin and/or Dr. Nick Bambos, may provide testimony as to the definition of the disputed terms as would be understood by one of ordinary skill in the relevant art and may provide an explanation of the technology.

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	rely on any statement made by any party under the Patent Local Rules.		
"**feedback**" found in claim numbers: '872 patent: 10 also presented for construction in: '094 patent: 21, 47	PROPOSED CONSTRUCTION: Information from output returned to the input DICTIONARY/TREATISE DEFINITIONS: Newton's Telecom Dictionary (17th ed. 2001): The return of part of an output signal back to the input side of the device; The American Heritage Dictionary of the English Language (4th ed. 2000): The return of a portion of the output of a process or system to the input, especially when used to maintain performance or to control a system or process; see also Dictionary of Computing (1st ed. 1983): Feedback queue: A form of scheduling mechanism often used in multiaccess systems. Individual processes are allocated a quantum of time on the processor. A process once started is allowed to run until it has exhausted its quantum, until it initiates a transfer on a peripheral device, or until an interrupt generated by some other process occurs. If the quantum is exhausted, the process is assigned a longer quantum and rejoins the queue. If the process initiates a transfer, its quantum remains unaltered and it rejoins the queue. If an externally generated interrupt occurs, the interrupt is serviced. Servicing the interrupt may free some other process already in the queue, in which case that process may be preferentially restarted;	PROPOSED CONSTRUCTION: Information derived from an output to adjust an input. REFERENCES: PATENT SPECIFICATION: The following citations support D-Link's proposed claim construction. "The transmit logic 39 also supplies status information across line 44 to the host interface logic 31, for posting to the host system. The status information includes indications of underrun conditions and may be *used by the host* to optimize the value in the threshold store 43." ('872; Col. 4: 56-60) (emphasis added). "The value for this register may be programmed by the host to optimize performance. If set too low, system latencies or bandwidth limitations may cause the adapter to underrun the network during transmission, causing a partial frame with a guaranteed bad CRC to be transmitted. If the value is set too high, then unnecessary delays will be incurred before the start of transmission. The adapter generates an indication of an underrun condition which is made available to the host through the XMIT FAILURE register. If such an underrun indication occurs, then the host driver should increase the value on	PROPOSED CONSTRUCTION: Information from output that is returned to input DICTIONARY/TREATISE DEFINITIONS: Webster's Ninth New Collegiate Dictionary (ninth edition, 1988) Feedback: 1. the return to the input of a part of the output of a machine, system, or process (as for producing changes in an electronic circuit that improve performance or in an automatic control device that provide self-corrective action.) The American Heritage Dictionary of the English Language (4th ed. 2000) The return of a portion of the output of a process or system to the input, especially when used to maintain performance or to control a system or process. IBM Dictionary of Computing (10th ed. 1993): The return of part of the output of a machine, process, or system as input to the computer, especially for self-correcting or control purposes. Microsoft Computer Dictionary (5th ed. 2002): The return of a portion of system output as input to the same system. . . .. Newton's' Telecom Dictionary (fourth edition, 1991) Feedback: The return of part

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	IBM Dictionary of Computing (10th ed. 1993): The return of part of the output of a machine, process, or system as input to the computer, especially for self-correcting or control purposes; Microsoft Computer Dictionary (5th ed. 2002): The return of a portion of system output as input to the same system. Often feedback is deliberately designed into a system, but sometimes it is unwanted. In electronics, feedback is used in monitoring, controlling, and amplifying circuitry. INTRINSIC EVIDENCE: Claims: see, e.g., claim 19; ("status information which may be used by the host system as feedback for optimizing the threshold value"); see also claim 10; Specification: see, e.g., figs. 2, 4, 13, 14, 17, 18; col. 2:31-34 ("the threshold value may be set by the host system to optimize performance using the alterable threshold store and the posted status information"); see also Col. 4: 56-60; Col. 29: 39-57; Col. 14: 53-57; Col. 19: 14-39; Col. 2: 27-34; see also Prosecution History: Office Action, Oct. 26, 1993, p. 5; Response to Office Action, Feb. 23, 1994, p. 2. EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of	the XMIT START THRESH register. Further underrun indications should cause the driver to continually increase the XMIT START THRESH value. If the XMIT START THRESH value is increased to a value of greater than the maximum length expected by the system, then the early transmit start features should be disabled by writing a zero to the XMIT START THRESH register." ('872; Col. 29: 39-57). "The XMIT FAILURE field contains the error code that is made up of the status bits gathered from the Ethernet transmitter after the completion of transmission. This field is mapped to the XMIT FAILURE register for host access." ('872; Col. 14: 53-57). "XMIT FAILURE returns the cause of a transmit failure. This register returns the cause of the failure of the attempt(s) to transmit a queued frame. A non-zero value indicates that the frame encountered one or more errors during the transmission attempt. The bits in this register are defined as follows: . . . bit 0 DMA UNDERRUN . . . This register will contain valid data regardless of the success or failure of the attempt to transmit a frame. If there was no failure, then this register will contain a value of 0 (hex). The contents of this register are valid after the frame has completed transmission (low byte of XMIT FRAME	of an output signal back to the input side of the device. Think of the high-pitched squeal you hear when someone brings a microphone too close to the loudspeaker. Not all feedback is as obvious or as irritating. Some feedback is good. Newton's Telecom Dictionary (17th ed. 2001): The return of part of an output signal back to the input side of the device. EXPERT TESTIMONY: Realtek's expert, Dr. Izhak Rubin, may provide testimony as to the definition of the disputed terms as would be understood by one of ordinary skill in the relevant art and may provide an explanation of the technology.

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action. See also U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and 6,570,884; Joint Claim Construction Statement in Cv-05-00098 (VRW). 3Com reserves the right to rely on any statement made by any party under the Patent Local Rules.	STATUS not equal to ff (hex)) and before XMIT PROT ID is read. If a data underrun occurs, the adapter will force a CRC error into the frame during transmission to assure that the frame is received as a bad frame and is discarded by the destination device." ('872; Col. 19: 14-39). "In one aspect of the invention, the monitoring logic includes a threshold store, which is programmable by the host computer for storing a threshold value and logic for posting status information to the host. Thus, the threshold value may be set by the host system to optimize performance using the alterable threshold store and the posted status information." ('872; Col. 2: 27-34). PROSECUTION HISTORY: Claim 10 of the '872 patent was amended to show feedback for use by the host system: ". . . control means, coupled with the network interface means, for posting status information [which may be used] for use by the host system, as feedback for optimizing the threshold value." ('872 prosecution history, Response mailed February 23, 1994, p. 2). EXTRINSIC EVIDENCE: *EXPERT TESTIMONY:* D-Link's expert, Howard Frazier, may provide	

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		testimony as to the definition of the disputed terms as would be understood by one of ordinary skill in the relevant art and may provide an explanation of the technology. *DICTIONARY/TREATISE DEFINITIONS:* Newton's Telecom Dictionary, 19th Ed., 2003, pg. 319: Feedback - "The return of part of an output signal back to the input side of the device." Webster's Ninth New Collegiate Dictionary, (1986), pg. 454: Feedback - "The return to the input of a part of the output of a machine, system, or process (as for producing changes in an electronic circuit that improve performance or in an automatic control device that provide self-corrective action)."	
"**optimizing the threshold**" found in claim numbers: '872 patent: 10 also presented for construction in: '094 patent: 21	PROPOSED CONSTRUCTION: Attempting to make the transmission of frames more efficient. DICTIONARY/TREATISE DEFINITIONS: See "**threshold value**" in subsection 1 for definitions of "threshold"; optimize: The American Heritage Dictionary of the English Language (4th ed. 2000): Optimize: Computer Science. To increase the computing speed and efficiency of (a program), as by rewriting instructions; see also Microsoft Computer Dictionary (5th	PROPOSED CONSTRUCTION: Adjusting the current threshold amount to make it as efficient, effective, or functional as possible. EXTRINSIC EVIDENCE: *DICTIONARY/TREATISE DEFINITIONS:* Webster's Third New International Dictionary Unabridged (1981): "to make as perfect, effective, or functional as possible." p.1585 WordNet 2.1 lexical database, Princeton Univ.	PROPOSED CONSTRUCTION: Dynamically changing the threshold value by the host system to make it as perfect, effective, or functional as possible. INTRINSIC EVIDENCE: '872 patent, Abstract; '094 patent, Abstract ("The monitoring logic includes *a threshold store, which is programmable by the host computer* for storing a threshold value. Thus, *the threshold value may be set by the host system to optimize performance in a given setting.*")

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	ed. 2002): Optimization: 1. In programming, the process of producing more efficient (smaller or faster) programs through selection and design of data structures. 2. The process of a compiler or assembler in producing efficient executable code. INTRINSIC EVIDENCE: Claims: claim 10; claim 19; Specification: figs. 2, 4, 13, 14, 17, 18; col. 29:35-38 ("If this register set to zero, then the early transmit feature is disabled and the entire transmit frame must reside on the adapter before the adapter will begin to transmit it"); col. 29:48-51 ("If such an underrun indication occurs, then the host driver should increase the value on the XMIT START THRESH register"); see also col. 29:12-57; col. 4:46-55; col. 2:27-34; col. 2:31-34; col. 4:58-60; col. 29:39-40; see also Prosecution History: Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 5; Part 131 Affidavit, p. Ex. 1, p. 6; Response to Office Action, Feb. 23, 1994, p. 2. EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action.	(1991-2005) at http://wordnet.princeton.edu/perl/webwn; make optimal; get the most out of; use best - 'optimize your resources'; modify to achieve maximum efficiency in storage capacity or time or cost - 'optimize a computer program'" D-Link also incorporates by reference Realtek's references.	'872 patent at 2:27-34; '094 patent at 2: 21-27 ("In one aspect of the invention, the monitoring logic includes *a threshold store, which is programmable by the host computer for storing a threshold value* and logic for posting status information to the host. Thus, *the threshold value may be set by the host system to optimize performance using the alterable threshold store* and the posted status information.") '872 patent at 4:46-55; '094 patent at 4:38-46 ("*The threshold store 43, in a preferred system, is dynamically programmable by the host computer 30.* In this embodiment, the threshold store 43 is a register accessible by the host through the interface logic 31. *Alternatively, the threshold store may be a read only memory set during manufacture.* In yet other alternatives, the threshold store *may be implemented using user specified data* in non-volatile memory, such as EEPROMs, FLASH EPROMs, or other memory storage devices.") '872 patent at 29:12-57; '094 patent at 27:44-28:-17 ("XMIT START THRESH is used to specify the number of bytes of the transmit frame that must reside on the adapter, . . ., before the adapter can commence with the media access control functions associated with transmitting the frame.

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	See also U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and 6,570,884; Joint Claim Construction Statement in Cv-05-00098 (VRW). 3Com reserves the right to rely on any statement made by any party under the Patent Local Rules.		. . . The value for this register *may be programmed by the host to optimize performance*. . . . The adapter generates an indication of an underrun condition which is made available to the host through the XMIT FAILURE register. If such an underrun indication occurs, then the host driver should increase the value on the XMIT START THRESH register. Further underrun indications should cause the driver to continually increase the XMIT START THRESH value. . . .") DICTIONARY/TREATISE DEFINITIONS: See "**altering the threshold**" for definitions of "threshold." Optimize: Webster's Ninth New Collegiate Dictionary, (ninth edition, 1988) Optimize: to make as perfect, effective, or functional as possible. EXPERT TESTIMONY: Realtek's expert, Dr. Izhak Rubin, may provide testimony as to the definition of the disputed terms as would be understood by one of ordinary skill in the relevant art and may provide an explanation of the technology.
"**threshold value**" found in claim numbers:	PROPOSED CONSTRUCTION: A value representing the quantity of data sufficient to trigger the initiation of	PROPOSED CONSTRUCTION: A set value indicating a desired limit.	PROPOSED CONSTRUCTION: A number corresponding to a level of data required for some process to take place.

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
'872 patent: 10 also presented for construction in: '459 patent: 1 '094 patent: 47	transmission DICTIONARY/TREATISE DEFINITIONS: See "**threshold value**" in subsection 1 for definitions of "threshold." INTRINSIC EVIDENCE: Claims: claim 5; claim 6; claim 10; claim 19; claim 23; claim 24; Specification: see, e.g., figs. 11-17; col. 2:22-27 ("The network interface controller includes logic for initiating transmission of the frame when the threshold determination indicates that a sufficient portion of the frame is resident in the transmit buffer, and prior to the transfer of all of the data of the frame into the transmit buffer."); see also col. 2:27-34; col. 4:40-45; col. 19:3-5; col. 26:6-9; col. 29:28-31; Col. 2: 49-55; Col. 21: 12-39; Col. 3: 59-65; Col. 4: 68-Col. 5: 13; Col. 4: 40-45; see also Prosecution History: Office Action, Oct. 26, 1993, p. 4; Office Action, Oct. 26, 1993, p. 5; Response to Office Action, Feb. 23, 1994, p. 2. EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action.	REFERENCES: PATENT SPECIFICATION: The following citations support D-Link's proposed claim construction. "Coupled with the *threshold* logic 36 is a *threshold* store 43 which stores a *threshold value* which indicates an amount of data of a frame that must be resident in the frame buffer 34 before transmission of that frame may be initiated by the transmit DMA logic and MAC 39." ('872; Col. 4: 40-45) (emphasis added). "When the *threshold amount* of data is resident in the buffer 34, then the transmit logic 39 is instructed to begin transmission of the frame. The transmit logic 39 then begins retrieving data from the buffer 34 to support transmission of the frame on the medium 42. This operation begins before the entire frame has been transferred from the host computer 30 into the buffer 34, if the transmit logic 39 is available to transmit the frame subject of the ongoing download from the host computer 30, the frame being downloaded into the buffer 34 is larger than the threshold set by the threshold store 43, and the host computer 30 indicates that immediate transmission of the data is desired." ('872; Col. 4: 68-Col. 5: 13) (emphasis added). "FIG. 1 illustrates a data communication system	DICTIONARY/TREATISE DEFINITIONS: threshold Webster's Ninth New Collegiate Dictionary (1983) Threshold - A level, point, or value above which something is true or will take place and below which it is not or will not. The American Heritage Dictionary of the English Language (4th ed. 2000) The point that must be exceeded to begin producing a given effect or result or to elicit a response. McGraw-Hill Electronics Dictionary (fifth edition, 1994) Threshold: 1. The least value of a current, voltage, or other quantity that produces the minimum detectable response. It is also called a limen. 2. The level of pumping at which a laser can go into self-excited oscillation. threshold value McGraw-Hill Electronics Dictionary (fifth edition, 1994) Threshold Value: The minimum input that produces a corrective action in an automatic control system. EXPERT TESTIMONY: Realtek's expert, Dr. Izhak Rubin, may provide testimony as to the definition of the disputed

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	See also U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and 6,570,884; Joint Claim Construction Statement in Cv-05-00098 (VRW). 3Com reserves the right to rely on any statement made by any party under the Patent Local Rules.	according to the present invention with a controller circuit using a dedicated transmit buffer memory which is automatically enabled to begin transmission of a frame on the network when the number of bytes available in the transmit buffer memory exceeds a preprogrammed *threshold*." ('872; Col. 3: 59-65) (emphasis added). "XMIT START THRESH provides for an early start of transmission. The XMIT START THRESH register is used to specify the number of transmit bytes that must reside on the adapter before it will start transmission. Values greater than the maximum frame length will prevent this function from operating properly. The method for disabling this function is to set the register to zero. Bytes are counted starting with the first byte of the destination field of the transmit frame. The number of bytes considered to be available is the sum of the immediate data written to XMIT AREA by the host and those bytes transferred to the transmit data buffers in the adapter using bus master DMA operations. The transmit request will be posted immediately after XMIT START THRESH transmit frame bytes are made available from the immediate data or when the adapter has bus-mastered XMIT START THRESH-XMIT IMMED LEN bytes onto the adapter. The number of bytes resident on the adapter must be equal to or greater than the value in	terms as would be understood by one of ordinary skill in the relevant art and may provide an explanation of the technology.

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		XMIT START THRESH for the transmission to commence, unless the total frame size is less than XMIT START THRESH. In that case, the frame will begin transmission when the entire frame has been copied to the adapter. The actual transmission of the frame may be delayed by previous pending transmit frames and by deferrals to network traffic. This register is set to zero during a reset." ('872; Col. 21: 12-39) "The *threshold logic* determines the amount of immediate data from the descriptor, and monitors the downloading of data of the frame into the download area. When the combination meets the *threshold*, then actual transmission of the frame is initiated. Thus, transmission of a frame may be initiated before the complete frame has been downloaded into the download area." ('872; Col. 2: 49-55) (emphasis added). *DICTIONARY/TREATISE DEFINITIONS:* Webster's Ninth New Collegiate Dictionary (1983), pg.229: Threshold - "A level, point, or value above which something is true or will take place and below which it is not or will not." *EXPERT TESTIMONY:* D-Link's expert, Howard Frazier, may provide testimony as to the definition of the disputed	

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		terms as would be understood by one of ordinary skill in the relevant art and may provide an explanation of the technology.	
"**logic which initiates transmission of the frame when no complete frame of data is present in the buffer memory**" found in claim numbers: '872 patent: 21	PROPOSED CONSTRUCTION: Threshold logic that begins transmission of a frame before all the data in the frame is within the buffer memory. DICTIONARY/TREATISE DEFINITIONS: See "**logic**," "**frame**" and "**buffer**" in subsection 1 for definitions of those terms, respectively, "**data value**" in subsection 6 for definitions of "data," and "**buffer memory**" in subsection 1 for definitions of "memory;" transmission: The American Heritage Dictionary of the English Language (4th ed. 2000): The act or process of transmitting. The fact of being transmitted. transmit: To pass along (news or information); communicate. initiate: The American Heritage Dictionary of the English Language (4th ed. 2000): To set going by taking the first step; begin: initiated trade with developing nations. See Synonyms at begin. To introduce to a new field, interest, skill, or activity. To admit into membership, as with ceremonies or ritual. Initiated or admitted, as to membership or a position of authority. Instructed in esoteric knowledge. Introduced to something new. One who is being or has been initiated. One who has been introduced to or has attained knowledge in a	Refer to the construction under 35 U.S.C. § 112 ¶ 6 in Section B.	Please refer to the construction under 35 U.S.C. § 112 ¶ 6. To the extent this term requires construction, Realtek asserts that "logic" should be construed as "means" and, therefore, this claim element should be governed by 35 U.S.C. § 112 ¶ 6. If the Court determines that 35 U.S.C. § 112 ¶ 6 does not apply, the claim limitation should be construed as "device that initiates transmission of the frame when no complete frame of data is present in the buffer memory."

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	particular field. INTRINSIC EVIDENCE: Claims: claim 1; claim 21; Specification: see, e.g., figs. 1, 2, 4, 4A, 5, 9, 11-18; col. 2:22-27 ("The network interface controller includes logic for initiating transmission of the frame when the threshold determination indicates that a sufficient portion of the frame is resident in the transmit buffer, and prior to the transfer of all of the data of the frame into the transmit buffer."); see also col. 4:40-45; see also Prosecution History: Part 131 Affidavit, pp. 2-3; Response to Office Action, Oct. 5, 1994, p. 2; Response to Office Action, Oct. 5, 1994, p. 3. EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action. See also U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and 6,570,884; Joint Claim Construction Statement in Cv-05-00098 (VRW). 3Com reserves the right to rely on any statement made by any party under the Patent Local Rules.		

3. U.S. Pat. No. 5,732,094

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
"**buffer**" found in claim numbers: '094 patent: 1, 9, 21, 28, 39, 47 also presented for construction in: '459 patent: 1 '872 patent: 1, 10, 21	PROPOSED CONSTRUCTION: A memory for temporary storage of data. DICTIONARY/TREATISE DEFINITIONS: See "**buffer**" in subsection 1. INTRINSIC EVIDENCE: Claims: see, e.g., claim 33 ("The method as in claim 28, wherein the initiating transmission of the frame step includes: retrieving data from the buffer memory; and supplying the retrieved data for transmission to the network transceiver."); see also claim 1; claim 4; claim 6; claim 7; claim 9; claim 10; claim 11; claim 14; claim 16; claim 20; claim 21; claim 28; claim 29; claim 30; claim 34; claim 38; claim 39; claim 41; claim 44; claim 45; claim 47; claim 49; claim 52; Specification: see, e.g., figs. 2, 6-10E; col. 1:44-50 ("Transmit data buffers are to be distinguished from first-in-first-out FIFO systems in which the sending system downloads data of a frame into the FIFO, while the network adapter unloads the FIFO during a transmission."); col. 2:28-30 ("the transmit data buffer includes a transmit descriptor ring, and a transmit data buffer") and other quotes from **"buffer"** in subsection 2 above, which also appear in the specification of the '094, since it is a continuation of the '872; see also col. 1:29-	PROPOSED CONSTRUCTION: Term is used only in phrase "buffer memory." See construction of "buffer memory."	Same as "**buffer memory**" identified above.

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	33; col. 1:35-37; col. 1:38-50; col. 1:51-56; col. 1:56-58; col. 1:60-62; col. 2:3-5; col. 2:7-9; col. 2:11-20; col. 2:35-39; col. 3:14-33; col. 4:55-5:12; col. 5:31-32; col. 5:45-47; col. 6:20-22; col. 8:31-33; col. 8:34-37; col. 8:44-46; col. 8:48-51; col. 8:53-56; col. 8:58-61; col. 8:66-9:3; col. 9:8-10; col. 9:33-35; col. 9:38-43; col. 9:50-54; col. 9:56-59; col. 10:50-53; col. 10:55-58; col. 10:65-67; col. 11:1-4; col. 11:23-25; col. 11:34-37; col., 12:4-8; col. 12:18-28; col. 12:30-36; col. 12:39-41; col. 12:44-52; col. 12:54-13:5; col. 13:9-11; col. 13:17-21; col. 13:39-47; col. 14:52-54; col. 14:57-59; col. 15:8-10; col. 15:16-18; col. 15:20-22; col. 15:24-27; col. 15:42-45; col. 15:48-52; col. 15:64-67; col. 16:11-14; col. 16:18-22; col. 16:23-33; col. 16:35-42; col. 16:44-48; col. 16:63-65; col. 17:6-9; col. 17:30-34; col. 17:51-52; col. 17:55-58; col. 18:47-50; col. 20:19-22; col. 20:39-41; col. 20:56-57; col. 20:63-66; col. 20:67-21:3; col. 21:15-18; col. 21:22-27; col. 21:39-45; col. 21:47-50; col. 21:59-64; col. 22:33-35; col. 22:38-41; col. 22:49-53; col. 23:13-18; col. 23:24-27; col. 23:25-28; col. 23:28-31; col. 23:33-37; col. 24:27-30; col. 27:16-19; col. 27:39-42; col. 27:57-61; see also Prosecution History: Specification as Filed, p. 52; Specification as Filed, p. 53; Specification as Filed, p. 54; Specification as Filed, p. 55; Specification as Filed, p. 56; Specification as Filed, p. 57; Preliminary Amendment, Mar. 3, 1995, p. 2; Preliminary Amendment, Mar. 3, 1995,		

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	p. 6; Office Action, Mar. 19, 1996, p. 2; Office Action, Mar. 19, 1996, p. 3; Office Action, Mar. 19, 1996, p. 4; Office Action, Mar. 19, 1996, p. 5; Office Action, Mar. 19, 1996, p. 6; Office Action, Mar. 19, 1996, p. 7; Office Action, Mar. 19, 1996, p. 8; Office Action, Jan. 7, 1997, p. 2; Response to Office Action, Apr. 7, 1997, pp. 1-2; Response to Office Action, Apr. 7, 1997, p. 5. EXTRINSIC EVIDENCE: See section I.A, supra (agreed upon definition for "buffer" in '625 and '884 patents); 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action. See also U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and 6,570,884; Joint Claim Construction Statement in Cv-05-00098 (VRW). 3Com reserves the right to rely on any statement made by any party under the Patent Local Rules.		
"**buffer memory**" found in claim numbers: '094 patent: 1, 9, 21, 28, 39, 47	PROPOSED CONSTRUCTION: A memory for temporary storage of data. DICTIONARY/TREATISE DEFINITIONS: See "**buffer memory**" in	PROPOSED CONSTRUCTION: Dedicated random access memory that (1) stores transmit data, (2) is distinct from a FIFO, (3) can always retransmit a frame of data without having to retrieve it	PROPOSED CONSTRUCTION: A memory that (1) stores frame data such that the frame data can be retrieved independently of the order in which the frame data were stored and the frame

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
also presented for construction in: '459 patent: 1 '872 patent: 1, 10, 21	subsection 1. INTRINSIC EVIDENCE: Claims: see, e.g., claim 33 ("The method as in claim 28, wherein the initiating transmission of the frame step includes: retrieving data from the buffer memory; and supplying the retrieved data for transmission to the network transceiver."); see also claim 1; claim 2; claim 4; claim 6; claim 7; claim 9; claim 10; claim 11; claim 14; claim 16; claim 20; claim 21; claim 28; claim 29; claim 30; claim 33; claim 34; claim 38; claim 39; claim 41; claim 44; claim 47; claim 49; claim 52; Specification: see, e.g., col. 1:44-50 ("Transmit data buffers are to be distinguished from first-in-first-out FIFO systems in which the sending system downloads data of a frame into the FIFO, while the network adapter unloads the FIFO during a transmission."); col. 2:28-30 ("the transmit data buffer includes a transmit descriptor ring, and a transmit data buffer") and other quotes from **"buffer"** in subsection 2 above, which also appear in the specification of the '094, since it is a continuation of the '872; see also col. 2:3-5; col. 2:28-52; col. 1:60-65; col. 1: 34-50; col. 1: 51-58; col. 1: 60-65; col. 1: 66 - col. 2:2; col. 12: 45-53; col. 12: 54-63; col. 12: 64 - col.13: 5; col. 2: 8-12; col.	from a host, and (4) is controlled independently of the host system. REFERENCES: PATENT SPECIFICATION: Claim 2 of the '872 patent, the parent of the '094 patent, recites "The apparatus of claim 1, wherein the *transmit buffer* includes . . ." (emphasis added). Claim 7 of the '872 patent, the parent of the '094 patent, recites "The apparatus of claim 1, wherein the *buffer* includes a transmit descriptor ring buffer and a transmit data buffer . . ." (emphasis added). "Early initiation of transmission of data in a network interface that includes a dedicated *transmit buffer* is provided in a system which includes logic for transferring frames of data composed by the host computer into the transmit buffer." ('872 Abstract and '094 Abstract)[3] (emphasis added). "The present invention provides for the early initiation of transmission of data in a network interface that includes a *dedicated transmit buffer*. The system includes logic for transferring frames of data composed by the host	data can always be retained and reused and can be accessed by the host system; and (2) is not a first-in-first-out (FIFO) system. INTRINSIC EVIDENCE: '872 patent at 1:47-54; '094 patent at 1:44-50 ("*Transmit data buffers are to be distinguished from first-in-first-out FIFO systems*, in which the sending system downloads data of a frame into the FIFO, while the network adapter unloads the FIFO during a transmission. *The data in FIFOs cannot be retained and reused by the media access control functions, or by the host, like data in transmit data buffers.*") '872 patent at 1:65-2:2; '094 patent at 1:60-65 ("Furthermore, the prior art systems which use transmit data buffers require the host or sending system to manage the transmit data buffer. A network interface controller transfers data from the host managed transmit data buffer using DMA techniques through a FIFO buffer in the interface controller and on to the network.") '872 patent at 2:7-10; '094 patent at 2:3-5 ("*It is desirable to provide the advantages of a transmit data buffer, while maintaining the communications throughput available from the simpler*

[3] Citations to the description of the '872 patent can also be found in the description of the related '094 patent; all citations to the '872 patent apply equally to the '094 patent.

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	3:50-52; col. 5:45-47; see also Prosecution History: Specification as Filed, p. 52; Specification as Filed, p. 54; Specification as Filed, p. 55; Specification as Filed, p. 56; Specification as Filed, p. 57; Preliminary Amendment, Mar. 3, 1995, p. 2; Preliminary Amendment, Mar. 3, 1995, p. 6; Office Action, Mar. 19, 1996, p. 2; Office Action, Mar. 19, 1996, p. 3; Office Action, Mar. 19, 1996, p. 4; Office Action, Mar. 19, 1996, p. 6; Office Action, Mar. 19, 1996, p. 7; Office Action, Jan. 7, 1997, p. 2; Response to Office Action, Apr. 7, 1997, pp. 1-2; Response to Office Action, Apr. 7, 1997, p. 5. EXTRINSIC EVIDENCE: See section I.A, supra (agreed upon definition for "buffer" in '625 and '884 patents). 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action. See also U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and 6,570,884; Joint Claim Construction Statement in Cv-05-00098 (VRW). 3Com reserves the right to rely on any statement made by any party under the Patent Local Rules.	computer into the transmit buffer." ('094; Col. 2: 8-12) (emphasis added). "According to another aspect of the present invention, the *transmit buffer* includes a transmit descriptor ring, and a transmit data buffer. The host system composes a frame by storing a transmit descriptor in the adapter managed transmit descriptor ring." ('094; Col. 2: 28-32) (emphasis added). "Some network adapter interfaces include dedicated *transmit buffers* into which a frame of data composed by the sending system can be downloaded by the sending system. The frame is then stored in the *transmit data buffer* until the media access control functions associated with transmitting the frame on the network have successfully transmitted the frame, or cancelled the frame transmission. If the frame transmission is cancelled, the data may be retained in the *transmit data buffer* until the sending system initiates a second attempt to transmit the frame. Transmit data buffers are to be distinguished from first-in-first-out FIFO systems, in which the sending system downloads data of a frame into the FIFO, while the network adapter unloads the FIFO during a transmission. The data in FIFOs cannot be retained and reused by the media access control functions, or by the host, like data in *transmit data buffers*." ('094; Col. 1: 34-	*FIFO based systems.*") '872 patent at 2:35-55; '094 patent at 2:28-52 ("According to another aspect of the present invention, the transmit buffer includes a transmit descriptor ring, and a transmit data buffer. . . .") '872 patent at 13:17-48; '094 patent at 12:44-13:5 ("A. Transmit Data Buffer The transmit data buffer occupies 3K bytes as mentioned above. This region is divided into two 1.5K buffers. Only the data that are downloaded to the adapter via bus master transfers are stored in these buffers. The controller will use both the contents of the transmit data buffer and the immediate data portion of the transmit descriptors, when encapsulating a frame for transmission. . . . The transmit buffers are shared by the download DMA logic and the transmit DMA logic. The transmit DMA logic may switch from buffer 0 to buffer 1 and back again freely. The only restriction being the availability of transmit data as defined by the transmit start threshold register. . . .") '872 patent, at 1:5-14 ("CROSS-REFERENCE TO RELATED APPLICATIONS The present application is related to copending U.S. patent application entitled NETWORK INTERFACE WITH HOST INDEPENDENT BUFFER

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		50) (emphasis added). "Although *transmit data buffers* enable a sending system to compose and download a frame into the *transmit data buffer*, and then attend to other tasks while the network adapter attempts to transmit the frame, it suffers the disadvantage that transmission of a frame is delayed until the entire frame has been downloaded into the buffer. Thus, *transmit data buffer* type systems improve host system efficiency at the expense of network throughput." ('094; Col. 1: 51-58) (emphasis added). "Furthermore, the prior art systems which use *transmit data buffers* require the host or sending system to manage the transmit data buffer. A network interface controller transfers data from the host managed transmit data buffer using DMA techniques through a FIFO buffer in the interface controller and on to the network." ('094; Col. 1: 60-65) (emphasis added). "Representative prior art systems include the National Semiconductor DP83932B, a systems-oriented network interface controller (SONIC) and the Intel 82586 local area network coprocessor." ('094; Col. 1: 66 - Col. 2:2). "The *transmit data buffer* occupies 3K bytes as mentioned above. This region is divided into two 1.5K buffers. Only the data	MANAGEMENT, application Ser. No. 07/921,519, filed 28 Jul. 1992, now U.S. Pat. No. 5,299,313, which was owned at the time of invention and is currently owned by the same assignee.") '459 patent, at 1:5-13 ("CROSS-REFERENCE TO RELATED APPLICATIONS The present application is related to copending U.S. patent application entitled NETWORK INTERFACE WITH HOST INDEPENDENT BUFFER MANAGEMENT, Ser. No. 07/921,519, filed Jul. 28, 1992, which was owned at the time of invention and is currently owned by the same assignee.") '459 patent, at 13:58-14:22 ("A. Transmit Data Buffer The transmit data buffer occupies 3K bytes as mentioned above. This region is divided into two 1.5K buffers. Only the data that are downloaded to the adapter via bus master transfers are stored in these buffers. The controller will use both the contents of the transmit data buffer and the immediate data portion of the transmit descriptors, when encapsulating a frame for transmission. . . . The transmit buffers are shared by the download DMA logic and the transmit DMA logic. The transmit DMA logic may switch from buffer 0 to buffer 1 and back again freely. The only restriction being the

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		that are downloaded to the adapter via bus master transfers are stored in these buffers. The controller will use both the contents of the *transmit data buffer* and the immediate data portion of the transmit descriptors, when encapsulating a frame for transmission. The adapter automatically alternates the use of the *buffers* after choosing the *buffer* closest to the base of the memory as the power up default." ('094; Col. 12: 45-53) (emphasis added). "The *transmit buffers* are shared by the download DMA logic and the transmit DMA logic. The transmit DMA logic may switch from buffer 0 to buffer 1 and back again freely. The only restriction being the availability of transmit data as defined by the transmit start threshold register. The transmit DMA module switches from one buffer to the other whenever it has completed a transmission. The buffer switch occurs regardless of whether or not the transmission was successful and regardless of whether or not bus master download data were used in the preceding transmission." ('094; Col. 12: 54-63) (emphasis added). "The download DMA module may only switch from one *buffer* to the other, if the *buffer* it is going to switch to is not being used by the transmit DMA module. Download DMA will attempt to switch from one *buffer* to another every time it completes processing	availability of transmit data as defined by the transmit start threshold register. The transmit DMA module switches from one buffer to the other whenever it has completed a transmission. The buffer switch occurs regardless of whether or not the transmission was successful and regardless of whether or not bus master download data were used in the preceding transmission. . . . ") DICTIONARY/TREATISE DEFINITIONS: The Network Interface Technical Guide, (First Edition, 1992) Buffer: A temporary storage area in random access memory where the NIC or computer stores information (usually while transmitting or receiving network traffic). EXPERT TESTIMONY: Realtek's expert, Dr. Izhak Rubin, may provide testimony as to the definition of the disputed terms as would be understood by one of ordinary skill in the relevant art and may provide an explanation of the technology. PRIOR ART: Datesheet for "82596CA High-Performance 32-Bit Local Area Network Coprocessor," November 1989, Intel Corp, pg. 2 ("Two large, independent FIFOs-128 bytes for Receive and 64 bytes for

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		of a transmit descriptor as described below, regardless of whether or not any bus master operations were called for in the preceding descriptor. However, it will not change to a *buffer* that is in use by the transmit DMA module." ('094; Col. 12: 64 - Col.13: 5) (emphasis added). "The *transmit data buffer* occupies 3K bytes as mentioned above. This region is divided into two 1.5K buffers. Only the data that are downloaded to the adapter via bus master transfers are stored in these buffers. The controller will use both the contents of the transmit data buffer and the immediate data portion of the transmit descriptors, when encapsulating a frame for transmission. The adapter automatically alternates the use of the buffers after choosing the buffer closest to the base of the memory as the power up default." ('459; Col. 13: 59-68) (emphasis added). PROSECUTION HISTORY: The following citation to the prosecution history of the parent '872 patent supports D-Link's proposed claim construction. During prosecution of the application that issued as the '872 patent, in a Response dated February 23, 1994, 3Com stated the following: "Accordingly, the Firoozmand, et al. reference does not initiate	Transmit-tolerate long bus latencies and provide programmable thresholds that allow the user to optimize bus overhead for any worst-case bus latency.") Datasheet for "The SUPERNET 2 Family for FDDI", October 1991, Advanced Micro Devices, Inc., pg. 2-37 ("The transmit FIFO (Figure 1) is a 36-bit by 9-word first-in-first-out register that temporarily stores data to be transmitted. In this way, continuity of data transmission is assured by providing a way to store a portion of the output data stream to compensate for delays involved in accessing the buffer memory.") 1992 Local Area Network Databook Including Datasheet For DP83932B Systems-Oriented Network Interface Controller (SONIC), 1992, National Semiconductor Corp, pg.1-295: ("The SONIC incorporates two independent 32-byte FIFOs for transferring data to/from the system interface and from/to the network. The FIFOs, providing temporary storage of data, free the host system from the real-time demands on the network.") Ethernet/IEEE-802.3 Family 1990 World Network Data Book/Handbook, Advanced Micro Devices, pg. 1-63, ("FIFO Operations The FIFO provides temporary buffer storage for

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		transmission to the network upon the threshold determination. Rather, transmission to the network is initiated only when there is a full frame available in the buffer. When the token has been received by the transmitting station, and it has a full frame for transmission, then a transmission process is begun. The transmission process continues, relying on the threshold determination to keep the pipeline full, only while the token is held by the transmitting station." "The environment is substantially different from the CSMA/CD network, which begins transmission to the medium access controller as soon as the threshold determination is met for an incoming frame. The MAC may succeed in transmitting the frame, may suffer collisions, or may suffer other types of errors which require backoff. Thus, the adapter as claimed in new claims 24-29, initiates transmission without being assured that the medium access controller is able to gain access to the communications medium. *This is a much more sophisticated control environment than that required by the FDDI system of Firoozmand, et al."* Response dated February 23, 1994, p. 5. EXTRINSIC EVIDENCE: *PRIOR ART:*	data being transferred between the parallel bus I/O pins and serial bus I/O pins. The capacity of the FIFO is 48 bytes. Transmit Data is loaded into the FIFO under internal micro-program control. The FIFO must be more than 16 bytes empty before the ILACC requests the bus (HOLD/BURREQ is asserted). The ILACC will start sending the preamble (if the line is idle) as soon as there is one byte loaded into the FIFO. Should the transmitter be required to back off, there will be up to 32 bytes of data in the FIFO ready for transmission. Reception has priority over transmission during the time that the transmitter is backing off. Receive Data is loaded into the FIFO from the serial input shift register during reception and leaves the FIFO under microprogram control. The ILACC microcode will wait until there are at least 16 bytes of data in the FIFO before initiating a DMA burst transfer. Preamble (including the synchronization bits) is not loaded into the FIFO.")

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		Datesheet for "82596CA High-Performance 32-Bit Local Area Network Coprocessor," November 1989, Intel Corp (Disclosed in D-Link's Preliminary Infringement Contentions), pg. 2: "Two large, independent FIFOs-128 bytes for Receive and 64 bytes for Transmit-tolerate long bus latencies and provide programmable thresholds that allow the user to optimize bus overhead for any worst-case bus latency." Datasheet for "The SUPERNET 2 Family for FDDI", October 1991, Advanced Micro Devices, Inc. (Disclosed in D-Link's Preliminary Infringement Contentions), pg. 2-37 : "The transmit FIFO (Figure 1) is a 36-bit by 9-word first-in-first-out register that temporarily stores data to be transmitted. In this way, continuity of data transmission is assured by providing a way to store a portion of the output data stream to compensate for delays involved in accessing the buffer memory." 1992 Local Area Network Databook Including Datasheet For DP83932B Systems-Oriented Network Interface Controller (SONIC), 1992, National Semiconductor Corp, pg.1-295: "The SONIC incorporates two independent 32-byte FIFOs for transferring data to/from the system interface and from/to the network. The FIFOs, providing temporary storage of data,	

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		free the host system from the real-time demands on the network." *DICTIONARY/TREATISE DEFINITIONS:* McGraw-Hill Illustrated Telecom Dictionary, Fourth Edition, 2001, pg. 83: Buffer - "A temporary storage (memory) device for data. A buffer is basically a box with RAM inside it. A common application for buffers is to collect a stream of data and temporarily store it until another device, such as a PC or server asks the buffer to download it. This is useful when the PC, server or LAN could be out of service for a period of time. When the server or PC is returned to service it just asks for the data from the buffer and it is downloaded. The buffer is then empty and ready to receive more data." *EXPERT TESTIMONY:* D-Link's expert, Howard Frazier, may provide testimony as to the definition of the disputed terms as would be understood by one of ordinary skill in the relevant art and may provide an explanation of the technology. D-Link also incorporates by reference Realtek's references.	
"**bad frame signal**" found in claim numbers:	PROPOSED CONSTRUCTION: A signal that a frame is bad. DICTIONARY/TREATISE DEFINITIONS:	PROPOSED CONSTRUCTION: A specific signal flag indicating that a corresponding frame contains invalid data.	PROPOSED CONSTRUCTION:: a signal indicating that a frame is bad. DICTIONARY/TREATISE

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
'094 patent: 21 also presented for construction in: '872 patent: 1	See "**bad frame signal**" in subsection 2. INTRINSIC EVIDENCE: Claims: claim 25 ("the bad frame signal includes a corrupted error detection code"); claim 4; claim 16; claim 21; claim 34; claim 41; Specification: fig. 18; col. 18:38-41; col. 27:7-9; col. 27:24-27; col. 27:27-35; col. 28:2-5; col. 27: 15-35 ; Fig. 18; see also Prosecution History: Specification as Filed, p. 53; Specification as Filed, p. 54; Specification as Filed, p. 56; Specification as Filed, p. 57; Specification as Filed, p. 58; Preliminary Amendment, Mar. 3, 1995, p. 6; Office Action, Mar. 19, 1996, p. 3; Response to Office Action, Apr. 7, 1997, p. 2. EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action. See also U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and 6,570,884; Joint Claim Construction Statement in Cv-05-00098 (VRW). 3Com reserves the right to rely on any statement made by any party under the Patent Local Rules.		DEFINITIONS: signal Newton's' Telecom Dictionary (fourth edition, 1991) Signal: 1. An electrical wave used to convey information 2. An alert. 3. An acoustic device (e.g. a bell) or a visual device (e.g. a lamp) which calls attention. To transmit an information signal or alerting signal. McGraw Hill Electronics Dictionary (fifth edition, 1994) Signal: Any variation in an electrical current, visible or nonvisible light, audible or ultrasonic energy that conveys information. Signals can be coded in frequency, phase, or amplitude to separate them from unwanted noise. bad: The American Heritage Dictionary of the English Language (4th Ed. 2000): adj. 1. Not achieving an adequate standard; poor: a bad concert. . . . 8. Injurious in effect; detrimental: bad habits. 9. Not working properly; defective: a bad telephone connection. 10. Full of or exhibiting faults or errors: bad grammar. INTRINSIC EVIDENCE: '872 patent at 28:48-29:2; '094 patent at 27: 15-35 ("According to the present invention, this transmit data path includes *an underrun detector 413* for detecting *a*

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
			condition in which the transferring of data into the transmit data buffer, . . ., by the host interface falls behind the transferring of data into the transmit data path 400 by the transmit DMA logic. . . . The underrun detector determines that a transmit write TXWR signal is not present during an expected interval of the frame transmission, *then a bad frame signal is generated on line 409.* . . .") '872 patent, Fig. 18; '094 patent, Fig. 18 ("a signal line identified as "bad frame" and connected "to host interface.") EXPERT TESTIMONY: Realtek's expert, Dr. Izhak Rubin, may provide testimony as to the definition of the disputed terms as would be understood by one of ordinary skill in the relevant art and may provide an explanation of the technology.
"**feedback**" found in claim numbers: '094 patent: 21, 47 also presented for construction in: '872 patent: 10	PROPOSED CONSTRUCTION: Information from output returned to the input DICTIONARY/TREATISE DEFINITIONS: See "**feedback**" in subsection 2. INTRINSIC EVIDENCE: Claims: see, e.g., claim 51 ("the step of altering the threshold value includes using a driver in the host system to process the status information, and in response write a new threshold value in a register on the network interface device"); see also claim 8; claim 13; claim 21;	PROPOSED CONSTRUCTION: Information derived from an output to adjust an input. REFERENCES: PATENT SPECIFICATION: The following citations support D-Link's proposed claim construction. "The transmit logic 39 also supplies status information across line 44 to the host interface logic 31, for posting to the host system. The status information includes indications of underrun conditions and	PROPOSED CONSTRUCTION: Information from output that is returned to input DICTIONARY/TREATISE DEFINITIONS: Webster's Ninth New Collegiate Dictionary (ninth edition, 1988) Feedback: 1. the return to the input of a part of the output of a machine, system, or process (as for producing changes in an electronic circuit that improve performance or in an automatic control device that provide self-corrective

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	claim 31; claim 46; claim 47; Specification: see, e.g., figs. 2, 4, 13, 14, 17, 18; col. 2:24-27 ("the threshold value may be set by the host system to optimize performance using the alterable threshold store and the posted status information"); see also Col. 2: 21-26; Col. 18: 20-41; Col. 14: 6-9; Col. 28: 1-17; Col. 4: 47-51; see also Prosecution History: Specification as Filed, p. 55; Specification as Filed, p. 58; Preliminary Amendment, Mar. 3, 1995, p. 6; Office Action, Mar. 19, 1996, p. 4; Response to Office Action, Apr. 7, 1997, p. 2. EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action. See also U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and 6,570,884; Joint Claim Construction Statement in Cv-05-00098 (VRW). 3Com reserves the right to rely on any statement made by any party under the Patent Local Rules.	may be *used by the host* to optimize the value in the threshold store 43." ('094; Col. 4: 47-51) (emphasis added). "The value for this register may be programmed by the host to optimize performance. If set too low, system latencies or bandwidth limitations may cause the adapter to underrun the network during transmission, causing a partial frame with a guaranteed bad CRC to be transmitted. If the value is set too high, then unnecessary delays will be incurred before the start of transmission. The adapter generates an indication of an underrun condition which is made available to the host through the XMIT FAILURE register. If such an underrun indication occurs, then the host driver should increase the value on the XMIT START THRESH register. Further underrun indications should cause the driver to continually increase the XMIT START THRESH value. If the XMIT START THRESH value is increased to a value of greater than the maximum length expected by the system, then the early transmit start features should be disabled by writing a zero to the XMIT START THRESH register." ('094; Col. 28: 1-17). "The XMIT FAILURE field contains the error code that is made up of the status bits gathered from the Ethernet transmitter after	action.) The American Heritage Dictionary of the English Language (4th ed. 2000) The return of a portion of the output of a process or system to the input, especially when used to maintain performance or to control a system or process. IBM Dictionary of Computing (10th ed. 1993): The return of part of the output of a machine, process, or system as input to the computer, especially for self-correcting or control purposes. Microsoft Computer Dictionary (5th ed. 2002): The return of a portion of system output as input to the same system. . . .. Newton's' Telecom Dictionary (fourth edition, 1991) Feedback: The return of part of an output signal back to the input side of the device. Think of the high-pitched squeal you hear when someone brings a microphone too close to the loudspeaker. Not all feedback is as obvious or as irritating. Some feedback is good. Newton's Telecom Dictionary (17th ed. 2001): The return of part of an output signal back to the input side of the device. EXPERT TESTIMONY: Realtek's expert, Dr. Izhak Rubin, may provide testimony as to the definition of the disputed

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		the completion of transmission. This field is mapped to the XMIT FAILURE register for host access." ('094; Col. 14: 6-9). "XMIT FAILURE returns the cause of a transmit failure. This register returns the cause of the failure of the attempt(s) to transmit a queued frame. A non-zero value indicates that the frame encountered one or more errors during the transmission attempt. The bits in this register are defined as follows: . . . bit 0 DMA UNDERRUN . . . This register will contain valid data regardless of the success or failure of the attempt to transmit a frame. If there was no failure, then this register will contain a value of 0 (hex). The contents of this register are valid after the frame has completed transmission (low byte of XMIT FRAME STATUS not equal to ff (hex)) and before XMIT PROT ID is read. If a data underrun occurs, the adapter will force a CRC error into the frame during transmission to assure that the frame is received as a bad frame and is discarded by the destination device." ('094; Col. 18: 20-41). "In one aspect of the invention, the monitoring logic includes a threshold store, which is programmable by the host computer for storing a threshold value and logic for posting status information to the host. Thus, the	terms as would be understood by one of ordinary skill in the relevant art and may provide an explanation of the technology.

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		threshold value may be set by the host system to optimize performance using the alterable threshold store and the posted status information." ('094; Col. 2: 21-26). PROSECUTION HISTORY: Claim 10 of the parent '872 patent was amended to show feedback for use by the host system: ". . . control means, coupled with the network interface means, for posting status information [which may be used] <u>for use</u> by the host system, as feedback for optimizing the threshold value." ('872 prosecution history, Response mailed February 23, 1994, p. 2). EXTRINSIC EVIDENCE: *DICTIONARY/TREATISE DEFINITIONS:* <u>Newton's Telecom Dictionary,</u> 19th Ed., 2003, pg. 319: Feedback - "The return of part of an output signal back to the input side of the device." <u>Webster's Ninth New Collegiate Dictionary,</u> (1986), pg. 454: Feedback - "The return to the input of a part of the output of a machine, system, or process (as for producing changes in an electronic circuit that improve performance or in an automatic control device that provide self-corrective action)."	

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		EXPERT TESTIMONY: D-Link's expert, Howard Frazier, may provide testimony as to the definition of the disputed terms as would be understood by one of ordinary skill in the relevant art and may provide an explanation of the technology.	
"**host system**" found in claim numbers: '094 patent: 1, 9, 21, 28, 39, 47 also presented for construction in: '459 patent: 1 '872 patent: 1, 10, 21 '884 patent: 1	PROPOSED CONSTRUCTION: A computer that communicates over a network DICTIONARY/TREATISE DEFINITIONS: Webster's New World Computer Dictionary (10th ed. 2003): 1. In the Internet, any computer that can function as the beginning and end point of data transfers. An Internet host has a unique Internet address (called an IP address) and a unique domain name. 2. In networks and telecommunications generally, a server that performs centralized functions, such as making program or data files available to other computers; The American Heritage Dictionary of the English Language (4th ed. 2000): Computer Science. A computer containing data or programs that another computer can access by means of a network or modem; Dictionary of Computing (3d ed. 1990): Host computer (host): A computer that is attached to a network and provides services other than simply acting as a store-and-	PROPOSED CONSTRUCTION: Any system or computer that communicates over a network Evidence (872: Col 1: lns. 65-67) (094: Col. 1, lns. 60-62) Furthermore, the prior art systems which use transmit data buffers require the *host or sending system* to manage the transmit data buffer. (872: Col. 3, ln. 65 to col. 4., ln. 2) ('094: Col. 3, lns. 59-64) As shown in FIG. 1, such system for communicating data includes a host data processing system, generally referred to by reference number 1, which includes a host system bus 2, a host central processing unit 3, host memory 4, and other host devices 5, all communicating across the bus 2 (884: Col. 2, lns. 39-44) The invention is particularly suited to environments in which the host system is actively handling communications and other	PROPOSED CONSTRUCTION: Any system or computer that communicates over a network Evidence (872: Col 1: lns. 65-67) (094: Col. 1, lns. 60-62) Furthermore, the prior art systems which use transmit data buffers require the *host or sending system* to manage the transmit data buffer. (872: Col. 3, ln. 65 to col. 4., ln. 2) ('094: Col. 3, lns. 59-64) As shown in FIG. 1, such system for communicating data includes a host data processing system, generally referred to by reference number 1, which includes a host system bus 2, a host central processing unit 3, host memory 4, and other host devices 5, all communicating across the bus 2 (884: Col. 2, lns. 39-44) The invention is particularly suited to environments in which the host system is actively handling communications and other

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	forward processor or communication switch. INTRINSIC EVIDENCE: Claims claim 1; claim 8; claim 9; claim 11; claim 12; claim 13; claim 17; claim 21; claim 22; claim 26; claim 28; claim 29; claim 30; claim 31; claim 35; claim 39; claim 46; claim 47; claim 51; Specification: see, e.g., col. 4:2-5 ("The network adapter 6 is, in turn, connected to an adapter memory 9, which is managed by the interface controller 6 or by the host CPU3"); see also col. 1:60-62; col. 1:45-48; col. 1:53-55; col. 1:57-59; col. 1:59-63; col. 2:9-11; col. 2:11-15; col. 2:20-23; col. 2:23-27; col. 2:29-31; col. 2:46-52; col. 2:63-1; col. 3:5-8; col. 3:8-10; col. 3:10-12; col. 3:55-64; col. 4:5-8; col. 4:8-10; col. 4:13-14; col. 4:18-21; col. 4:21-23; col. 4:23-25; col. 4:25-27; col. 4:38-39; col. 4:39-41; col. 4:47-49; col. 4:49-52; col. 4:52-53; col. 4:53-55; col. 4:55-57; col. 4-5:53-4; col. 5:4-9; col. 5:9-13; col. 5:18-21; col. 5:21-23; col. 5:23-26; col. 5:39-42; col. 5:45-47; col. 5:50-52; col. 6:12-14; col. 6:20-22; col. 6:34-36; col. 6-7:67-3; col. 7:39-43; col. 7:43-47; col. 7:51-53; col. 7:54-59; col. 8:4-5; col. 8:18-22; col. 8:30-32; col. 8:38-43; col. 9:38-41; col. 9:41-47; col. 9:50-52; col. 9:59-63; col. 9:63-66; col. 9-10:66-3; col. 10:3-6; col. 10:11-13; col. 10:27-30; col. 11:8-12; col. 11:12-14; col. 11:14-15; col. 11:15-18; col. 11:18-19; col. 11:19-21; col. 11:27-31; col. 11:31-34; col. 11:34-37; col. 11:44-46; col.	processing tasks, and in which the adapter is able to take over some specialized tasks without interfering with the active processing in the host system.	processing tasks, and in which the adapter is able to take over some specialized tasks without interfering with the active processing in the host system.

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	11:46-52; col. 11:52-53; col. 11:53-57; col. 11:62-66; col. 11-12:66-1; col. 12:1-2; col. 12:2-4; col. 12:10-11; col. 12:18-21; col. 12:21-24; col. 12:24-29; col. 12:29-30; col. 13:14-17; col. 13:22-26; col. 13:26-28; col. 13:51-54; col. 13:57-61; col. 14:2-6; col. 14:8-10; col. 14:14-16; col. 14:16-18; col. 14:18-21; col. 14:27-30; col. 14:36-37; col. 14:37-42; col. 14:42-43; col. 14:43-45; col. 14:45-48; col. 14:51-53; col. 14:53-56; col. 14:58-60; col. 14:62-64; col. 15:8-10; col. 15:10-13; col. 15:16-18; col. 15:20-21; col. 15:24-27; col. 15:27-28; col. 15:28-36; col. 15:38-41; col. 15:42-45; col. 15:45-47; col. 15:48-53; col. 15:64-1; col. 16:1-2; col. 16:2-5; col. 16:5-7; col. 16:7-11; col. 16:11-14; col. 16:25-30; col. 16:44-49; col. 16:49-51; col. 16:51-56; col. 16:59-63; col. 16-17:66-1; col. 17:10-11; col. 17:15-18; col. 17:27-30; col. 17:30-34; col. 17:48-51; col. 17:53-55; col. 17:59-63; col. 18:10-12; col. 18:54-58; col. 19:14-17; col. 19:38-41; col. 19:61-64; col. 19-20:67-1; col. 20:5-9; col. 20:19-22; col. 20:46-47; col. 20:47-51; col. 20:58-60; col. 20:60-63; col. 20:63-67; col. 21:7-10; col. 21:10-11; col. 21:22-28; col. 21:28-29; col. 21:29-33; col. 21:33-34; col. 21:53-55; col. 21:55-58; col. 22:5-6; col. 23:33-38; col. 24:8-12; col. 24:27-30; col. 24:31-39; col. 24:54-55; col. 25:39-43; col. 26:7-9; col. 27:16-21; col. 28:1-2; col. 28:7-9; col. 28:9-11; see also Prosecution History: Specification as Filed, p. 52; Specification as Filed, p. 52; Specification as Filed, p. 55; Specification as Filed, p. 55;		

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	Specification as Filed, p. 56; Specification as Filed, p. 57; Specification as Filed, p. 58; Preliminary Amendment, Mar. 3, 1995, p. 2; Preliminary Amendment, Mar. 3, 1995, p. 2; Preliminary Amendment, Mar. 3, 1995, p. 6; Office Action, Mar. 19, 1996, p. 2; Office Action, Mar. 19, 1996, p. 2; Office Action, Mar. 19, 1996, p. 2; Office Action, Mar. 19, 1996, pp. 2-3; Office Action, Mar. 19, 1996, p. 3; Office Action, Mar. 19, 1996, p. 4; Office Action, Mar. 19, 1996, p. 4; Office Action, Mar. 19, 1996, p. 4; Office Action, Mar. 19, 1996, p. 5; Office Action, Mar. 19, 1996, p. 6; Office Action, Mar. 19, 1996, pp. 6-7; Office Action, Mar. 19, 1996, p. 7; Office Action, Mar. 19, 1996, p. 7; Office Action, Mar. 19, 1996, p. 8; Office Action, Mar. 19, 1996, p. 8; Office Action, Jan. 7, 1997, p. 2; Response to Office Action, Apr. 7, 1997, pp. 1-2; Response to Office Action, Apr. 7, 1997, p. 2; Response to Office Action, Apr. 7, 1997, p. 5; Response to Office Action, Apr. 7, 1997, p. 5; Response to Office Action, Apr. 7, 1997, p. 5; Response to Office Action, Apr. 7, 1997, p. 5; Response to Office Action, Apr. 7, 1997, p. 5; Response to Office Action, Apr. 7, 1997, p. 5 <u>EXTRINSIC EVIDENCE</u>: 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a		

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action. See also U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and 6,570,884; Joint Claim Construction Statement in Cv-05-00098 (VRW). 3Com reserves the right to rely on any statement made by any party under the Patent Local Rules.		
"**optimizing the threshold**" found in claim numbers: '094 patent: 21 also presented for construction in: '872 patent: 10	PROPOSED CONSTRUCTION: Attempting to make the transmission of frames more efficient. DICTIONARY/TREATISE DEFINITIONS: See "**optimizing the threshold**" in subsection 2. INTRINSIC EVIDENCE: Claims see claim 8; claim 13; claim 21; claim 31; claim 46; claim 48; Specification: see, e.g., figs. 2, 4, 13, 14, 17, 18; col. 2:24-27 ("the threshold value may be set by the host system to optimize performance using the alterable threshold store and the posted status information"); col. 4:38-41; col. 4:49-51; col. 28:1-2; col. 27:65-67; col. 4:38-46 ; col. 2: 21-27 ; col. 27:44-28:-17; see also Prosecution History: Specification as Filed, p. 55; Specification as Filed, p. 58; Preliminary Amendment, Mar. 3, 1995, p. 6; Office Action, Mar. 19, 1996, p. 4; Response to Office Action,	PROPOSED CONSTRUCTION: Adjusting the current threshold amount to make it as efficient, effective, or functional as possible. REFERENCES: EXTRINSIC EVIDENCE: *DICTIONARY/TREATISE DEFINITIONS:* Webster's II New College Dictionary (1999): optimize: 1. To improve or develop as far as possible. 2. To make the most effective use of. WordNet 2.1 lexical database, Princeton Univ. (1991-2005) at http://wordnet.princeton.edu /perl/webwn make optimal; get the most out of; use best - 'optimize your resources'; modify to achieve maximum efficiency in storage capacity or time or cost - 'optimize a computer program'"	PROPOSED CONSTRUCTION: Dynamically changing the threshold value by the host system to make it as perfect, effective, or functional as possible. INTRINSIC EVIDENCE: '872 patent, Abstract; '094 patent, Abstract ("The monitoring logic includes *a threshold store, which is programmable by the host computer* for storing a threshold value. Thus, *the threshold value may be set by the host system to optimize performance in a given setting.*") '872 patent at 2:27-34; '094 patent at 2: 21-27 ("In one aspect of the invention, the monitoring logic includes *a threshold store, which is programmable by the host computer for storing a threshold value* and logic for posting status information to the host. Thus, *the threshold value may be set by the host system to optimize*

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	Apr. 7, 1997, p. 2. EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action. See also U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and 6,570,884; Joint Claim Construction Statement in Cv-05-00098 (VRW). 3Com reserves the right to rely on any statement made by any party under the Patent Local Rules.	*EXPERT TESTIMONY:* D-Link's expert, Howard Frazier, may provide testimony as to the definition of the disputed terms as would be understood by one of ordinary skill in the relevant art and may provide an explanation of the technology. D-Link also incorporates by reference Realtek's references.	*performance using the alterable threshold store* and the posted status information.") '872 patent at 4:46-55; '094 patent at 4:38-46 ("*The threshold store 43, in a preferred system, is dynamically programmable by the host computer 30.* In this embodiment, the threshold store 43 is a register accessible by the host through the interface logic 31. *Alternatively, the threshold store may be a read only memory set during manufacture.* In yet other alternatives, the threshold store *may be implemented using user specified data* in non-volatile memory, such as EEPROMs, FLASH EPROMs, or other memory storage devices.") '872 patent at 29:12-57; '094 patent at 27:44-28:-17 ("XMIT START THRESH is used to specify the number of bytes of the transmit frame that must reside on the adapter, . . ., before the adapter can commence with the media access control functions associated with transmitting the frame. . . . The value for this register *may be programmed by the host to optimize performance*. . . . The adapter generates an indication of an underrun condition which is made available to the host through the XMIT FAILURE register. If such an underrun indication occurs, then the host driver should increase the value on the XMIT

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
			START THRESH register. Further underrun indications should cause the driver to continually increase the XMIT START THRESH value. . . .") DICTIONARY/TREATISE DEFINITIONS: See "**altering the threshold**" for definitions of "threshold." Optimize: Webster's Ninth New Collegiate Dictionary, (ninth edition, 1988) Optimize: to make as perfect, effective, or functional as possible. EXPERT TESTIMONY: Realtek's expert, Dr. Izhak Rubin, may provide testimony as to the definition of the disputed terms as would be understood by one of ordinary skill in the relevant art and may provide an explanation of the technology.
"**threshold amount of data**" found in claim numbers: '094 patent: 21	PROPOSED CONSTRUCTION: A value representing the quantity of data sufficient to trigger the initiation of transmission DICTIONARY/TREATISE DEFINITIONS: See "**threshold value**" in subsection 1 for definitions of "threshold" and "**data value**" in subsection 6 for definitions of "data." INTRINSIC EVIDENCE: Claims: claim 7; claim 8; claim 9; claim 10; claim 12; claim 13; claim 15; claim	PROPOSED CONSTRUCTION: The amount of data required for some process to take place. REFERENCES: PATENT SPECIFICATION: The following citations support D-Link's proposed claim construction. "Coupled with the *threshold* logic 36 is a *threshold* store 43 which stores a *threshold value*	PROPOSED CONSTRUCTION: The amount of data required for some process to take place. DICTIONARY/TREATISE DEFINITIONS: threshold The American Heritage Dictionary of the English Language (4th ed. 2000): The point that must be exceeded to begin producing a given effect or result or to elicit a response.

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	21; claim 22; claim 23; claim 28; claim 30; claim 31; claim 32; claim 45; claim 46; claim 47; claim 48; claim 49; claim 50; claim 51; claim 53; Specification: see, e.g., figs. 11-17; col. 2:15-21 ("The network interface controller includes logic for initiating transmission of the frame when the threshold determination indicates that a sufficient portion of the frame is resident in the transmit buffer, and prior to the transfer of all of the data of the frame into the transmit buffer"); see also col. 2:10-12; col. 2:20-26; col. 2:39-43; col. 2:41-45; col. 3:26-29; col. 3:50-52; col. 4:8-11; col. 4:23-33; col. 4:38-46; col. 4:49-51; col. 4:57-61; col. 4:53-5:3; col. 12:57-58; col. 18:10-12; col. 21:3-4; col. 23:33-37; col. 23:45-49; col. 23:58-69; col. 24:1-3; col. 24:52-54; col. 25:53-55; col. 27:57-63; col. 2: 40-46; col. 20: 10-36; FIG. 1; col. 4: 59- 5: 3; col. 4: 32-37; col. 3:54-59; see also Prosecution History: Specification as Filed, p. 52; Specification as Filed, p. 53; Specification as Filed, p. 55; Specification as Filed, p. 56; Specification as Filed, p. 57; Specification as Filed, p. 58; Preliminary Amendment, Mar. 3, 1995, p. 6; Office Action, Mar. 19, 1996, p. 4; Office Action, Mar. 19, 1996, pp. 6-7; Office Action, Mar. 19, 1996, pp. 7-8; Response to Office Action, Apr. 7, 1997, p. 2. EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other	which indicates an amount of data of a frame that must be resident in the frame buffer 34 before transmission of that frame may be initiated by the transmit DMA logic and MAC 39." ('094; Col. 4: 32-37) (emphasis added). "When the *threshold amount* of data is resident in the buffer 34, then the transmit logic 39 is instructed to begin transmission of the frame. The transmit logic 39 then begins retrieving data from the buffer 34 to support transmission of the frame on the medium 42. This operation begins before the entire frame has been transferred from the host computer 30 into the buffer 34, if the transmit logic 39 is available to transmit the frame subject of the ongoing download from the host computer 30, the frame being downloaded into the buffer 34 is larger than the threshold set by the threshold store 43, and the host computer 30 indicates that immediate transmission of the data is desired." ('094; Col. 4: 59-Col. 5: 3) (emphasis added). "FIG. 1 illustrates a data communication system according to the present invention with a controller circuit using a dedicated transmit buffer memory which is automatically enabled to begin transmission of a frame on the network when the number of bytes available in the transmit buffer memory exceeds a preprogrammed	McGraw-Hill Electronics Dictionary (fifth edition, 1994) Threshold: 1. The least value of a current, voltage, or other quantity that produces the minimum detectable response. It is also called a limen. 2. The level of pumping at which a laser can go into self-excited oscillation. threshold value McGraw-Hill Electronics Dictionary (fifth edition, 1994) Threshold Value: The minimum input that produces a corrective action in an automatic control system. EXPERT TESTIMONY: Realtek's expert, Dr. Izhak Rubin, may provide testimony as to the definition of the disputed terms as would be understood by one of ordinary skill in the relevant art and may provide an explanation of the technology.

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action. See also U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and 6,570,884; Joint Claim Construction Statement in Cv-05-00098 (VRW). 3Com reserves the right to rely on any statement made by any party under the Patent Local Rules.	*threshold*." ('094; Col. 3: 54-59) (emphasis added). "XMIT START THRESH provides for an early start of transmission. The XMIT START THRESH register is used to specify the number of transmit bytes that must reside on the adapter before it will start transmission. Values greater than the maximum frame length will prevent this function from operating properly. The method for disabling this function is to set the register to zero. Bytes are counted starting with the first byte of the destination field of the transmit frame. The number of bytes considered to be available is the sum of the immediate data written to XMIT AREA by the host and those bytes transferred to the transmit data buffers in the adapter using bus master DMA operations. The transmit request will be posted immediately after XMIT START THRESH transmit frame bytes are made available from the immediate data or when the adapter has bus-mastered XMIT START THRESH-XMIT IMMED LEN bytes onto the adapter. The number of bytes resident on the adapter must be equal to or greater than the value in XMIT START THRESH for the transmission to commence, unless the total frame size is less than XMIT START THRESH. In that case, the frame will begin transmission when the entire frame has been copied to the adapter. The actual transmission of the frame may be delayed by previous	

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		pending transmit frames and by deferrals to network traffic. This register is set to zero during a reset." ('094; Col. 20: 10-36) "The *threshold logic* determines the amount of immediate data from the descriptor, and monitors the downloading of data of the frame into the download area. When the combination meets the *threshold*, then actual transmission of the frame is initiated. Thus, transmission of a frame may be initiated before the complete frame has been downloaded into the download area." ('094; Col. 2: 40-46) (emphasis added). "If host processor 5 responds to network adapter 3 before a complete data frame is transferred, host processor 5 then may decrease the *threshold value* in alterable storage location 10a enabling threshold logic 10 to generate the indication signal at a later time in the next transfer of a data frame. Alternatively, if host processor 5 responds to the network adapter 3 after a complete data frame has already been transferred, host processor 5 may then increase the threshold value in alterable storage location 10a enabling the threshold logic to generate an indication signal at an earlier time in the next transfer of a data frame." ('459; Col. 6: 48-59) (emphasis added).	

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		EXTRINSIC EVIDENCE: *DICTIONARY/TREATISE DEFINITIONS:* Webster's Ninth New Collegiate Dictionary (1983), pg.229: Threshold - "A level, point, or value above which something is true or will take place and below which it is not or will not." *EXPERT TESTIMONY:* D-Link's expert, Howard Frazier, may provide testimony as to the definition of the disputed terms as would be understood by one of ordinary skill in the relevant art and may provide an explanation of the technology.	
"**underrun**" found in claim numbers: '094 patent: 21 also presented for construction in: '872 patent: 1	PROPOSED CONSTRUCTION: When expected data from a frame to be transferred is not available DICTIONARY/TREATISE DEFINITIONS: See "**underrun**" in subsection 2. INTRINSIC EVIDENCE: Claims: see, e.g., claim 8 ("The method as in claim 7, further comprising: providing access to the threshold value so that it may be dynamically programmed by the host system; and posting status information for use by the host system as feedback for optimizing the threshold value."); claim 22 ("The method as in claim 21, wherein the threshold amount is dynamically programmable by the host	PROPOSED CONSTRUCTION: The condition of falling behind. See construction for "falls behind."	PROPOSED CONSTRUCTION: A condition in which the transferring of data into a transmit data buffer by the host interface falls behind the transferring of data into a transmit data path by a transmit logic. INTRINSIC EVIDENCE: '872 patent at 28:48-29:2 ("According to the present invention, this transmit data path includes an underrun detector 413 for detecting a condition in which the transferring of data into the transmit data buffer, or immediate data to the transmit descriptor buffer, by the host interface falls behind the transferring of data into the transmit data path 400 by the transmit DMA logic. . . . The

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	computer."); claim 30 ("The method as in claim 28, wherein the threshold determination is based on a comparison of the amount of data transferred into the buffer memory with a threshold value, the threshold value being dynamically programmable by the host system."); see also claim 4; claim 6; claim 16; claim 20; claim 21; claim 34; claim 38; claim 41; claim 44; claim 52; claim 53; Specification: see, e.g., fig. 18; col. 4:50-52; col. 7:62-4; col. 9:11-13; col. 14:22-23; col. 18:26-30; col. 22:10-12; col. 26:60-61; col. 27:16-21; col. 27:21-23; col. 27:25-32; col. 27:34-36; col. 28:2-5; col. 28:7-17; see also Prosecution History: Specification as Filed, p. 53; Specification as Filed, p. 54; Specification as Filed, p. 56; Specification as Filed, p. 57; Specification as Filed, p. 58; Preliminary Amendment, Mar. 3, 1995, p. 6; Office Action, Mar. 19, 1996, p. 3; Response to Office Action, Apr. 7, 1997, p. 2. EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action. See also U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and		underrun detector determines that a transmit write TXWR signal is not present during an expected interval of the frame transmission, then a bad frame signal is generated on line 409. . . . ") EXPERT TESTIMONY: Realtek's expert, Dr. Izhak Rubin, may provide testimony as to the definition of the disputed terms as would be understood by one of ordinary skill in the relevant art and may provide an explanation of the technology.

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	6,570,884; Joint Claim Construction Statement in Cv-05-00098 (VRW). 3Com reserves the right to rely on any statement made by any party under the Patent Local Rules.		
"**altering** the threshold" found in claim numbers: '094 patent: 47	PROPOSED CONSTRUCTION: changing DICTIONARY/TREATISE DEFINITIONS: See "**alterable storage location**" in subsection 1 for definitions of "alter" and "**threshold value**" in subsection 1 for definitions of "threshold." INTRINSIC EVIDENCE: Claims: see, e.g., claim 49 ("including allowing alteration of the threshold value while data of a frame to be transmitted is stored in the buffer memory"); see also claim 47; claim 48; claim 50; claim 51; claim 53; Specification: see, e.g., figs. 2, 4, 13, 14, 17, 18; col. 4:38-39 ("The threshold store 43, in a preferred system, is dynamically programmable by the host computer 30"); col. 4:43-46 ("In yet other alternatives, the threshold store may be implemented using user specified data in non-volatile memory, such as EEPROMs, FLASH EPROMs, or other memory storage devices."); see also col. 2:23-26; col. 4:38-41; col. 28:1-17; col. 4:38-46; col. 2:21-27; col. 27:44-28:17; see also Prosecution History: Specification as Filed, p. 52; Specification as Filed, p. 55; Specification as Filed, p. 58.	PROPOSED CONSTRUCTION: dynamically changing REFERENCES: PATENT SPECIFICATION: The following citations support D-Link's proposed claim construction: "The threshold store 43, in a preferred system, is *dynamically programmable* by the host computer 30. In this embodiment, the threshold store 43 is a register accessible by the host through the interface logic 31." ('094; Col. 4: 38-41). "The value for this register may be programmed by the host to optimize performance. If set too low, system latencies or bandwidth limitations may cause the adapter to underrun the network during transmission, causing a partial frame with a guaranteed bad CRC to be transmitted. If the value is set too high, then unnecessary delays will be incurred before the start of transmission. The adapter generates an indication of an underrun condition which is made available to the host through the XMIT FAILURE register. If such an underrun indication occurs, then the host driver	PROPOSED CONSTRUCTION: dynamically changing INTRINSIC EVIDENCE: '094 patent, Abstract ("The monitoring logic includes a threshold store, which is *programmable by the host computer* for storing a threshold value. Thus, *the threshold value may be set by the host system to optimize performance in a given setting.*") '094 patent at 4:38-46 ("*The threshold store 43, in a preferred system, is dynamically programmable by the host computer 30*. In this embodiment, the threshold store 43 is a register accessible by the host through the interface logic 31. *Alternatively, the threshold store may be a read only memory set during manufacture*. In yet other alternatives, the threshold store may be implemented using user specified data in non-volatile memory, such as EEPROMs, FLASH EPROMs, or other memory storage devices.") '094 patent at 2: 21-27 ("In one aspect of the invention, *the monitoring logic includes a threshold store, which is programmable by the host computer* for storing a threshold value

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action. See also U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and 6,570,884; Joint Claim Construction Statement in Cv-05-00098 (VRW). 3Com reserves the right to rely on any statement made by any party under the Patent Local Rules.	should increase the value on the XMIT START THRESH register. Further underrun indications should cause the driver to continually increase the XMIT START THRESH value. If the XMIT START THRESH value is increased to a value of greater than the maximum length expected by the system, then the early transmit start features should be disabled by writing a zero to the XMIT START THRESH register." ('094; Col. 28: 1-17). "If host processor 5 responds to network adapter 3 before a complete data frame is transferred, host processor 5 then may decrease the threshold value in *alterable storage location* 10a enabling threshold logic 10 to generate the indication signal at a later time in the next transfer of a data frame. Alternatively, if host processor 5 responds to the network adapter 3 after a complete data frame has already been transferred, host processor 5 may then increase the threshold value in alterable storage location 10a enabling the threshold logic to generate an indication signal at an earlier time in the next transfer of a data frame." ('459; Col. 6: 48-59). *DICTIONARY/TREATISE DEFINITIONS:* Webster's II New College Dictionary (2001), pg. 33: Altering – "To make different."	and logic for posting status information to the host. Thus, *the threshold value may be set by the host system to optimize performance using the alterable threshold store* and the posted status information.") '094 patent at 27:44-28:17 ("XMIT START THRESH is used to specify the number of bytes of the transmit frame that must reside on the adapter, . . . , before the adapter can commence with the media access control functions associated with transmitting the frame. . . . The value for this register *may be programmed by the host to optimize performance*. If set too low, system latencies or bandwidth limitations may cause the adapter to underrun the network during transmission, causing a partial frame with a guaranteed bad CRC to be transmitted. If the value is set too high, then unnecessary delays will be incurred before the start of transmission. . . .") DICTIONARY/TREATISE DEFINITIONS: Webster's Ninth New Collegiate Dictionary (Ninth Edition, 1988) Alter: 1: to make different without changing into something else 2: CASTRATE SPAY ~ vi: to become different syn see CHANGE; alterable – adj. The American Heritage Dictionary of the English

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		EXPERT TESTIMONY: D-Link's expert, Howard Frazier, may provide testimony as to the definition of the disputed terms as would be understood by one of ordinary skill in the relevant art and may provide an explanation of the technology. D-Link also incorporates by reference Realtek's references.	Language (4th Ed. 2000) alter: v. tr. To change or make different; modify: altered my will. intr. To change or become different. threshold Webster's Ninth New Collegiate Dictionary (1983) Threshold - A level, point, or value above which something is true or will take place and below which it is not or will not. The American Heritage Dictionary of the English Language (4th ed. 2000) The point that must be exceeded to begin producing a given effect or result or to elicit a response. McGraw-Hill Electronics Dictionary (fifth edition, 1994) Threshold: 1. The least value of a current, voltage, or other quantity that produces the minimum detectable response. It is also called a limen. 2. The level of pumping at which a laser can go into self-excited oscillation. EXPERT TESTIMONY: Realtek's expert, Dr. Izhak Rubin, may provide testimony as to the definition of the disputed terms as would be understood by one of ordinary skill in the relevant art and may provide an explanation of the technology.
"**threshold value**" found in claim	PROPOSED CONSTRUCTION: A value representing the quantity of data sufficient to	PROPOSED CONSTRUCTION: A set value indicating a desired limit.	PROPOSED CONSTRUCTION: A number corresponding to a level of data required for

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
numbers: '094 patent: 47 also presented for construction in: '459 patent: 1 '872 patent: 10	trigger the initiation of transmission DICTIONARY/TREATISE DEFINITIONS: See "**threshold value**" in subsection 1. INTRINSIC EVIDENCE: Claims: claim 7; claim 8; claim 30; claim 31; claim 32; claim 45; claim 46; claim 47; claim 48; claim 49; claim 50; claim 51; claim 53; Specification: see, e.g., figs. 11-17col. 2:15-21 ("The network interface controller includes logic for initiating transmission of the frame when the threshold determination indicates that a sufficient portion of the frame is resident in the transmit buffer, and prior to the transfer of all of the data of the frame into the transmit buffer"); see also col. 2:20-26; col. 4:32-37; col. 4:49-51; col. 18:10-12; col. 23:43-47; col. 23:56-67; col. 24:1-3; col. 24:52-54; col. 27:61-63; col. 4:59- 5:3; col. 3:54-59; col. 20:10-36; 2:40-46; see also Prosecution History: Specification as Filed, p. 52; Specification as Filed, p. 53; Specification as Filed, p. 55; Specification as Filed, p. 58; Office Action, Mar. 19, 1996, p. 4. EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term.	REFERENCES: PATENT SPECIFICATION: The following citations support D-Link's proposed claim construction. "Coupled with the *threshold* logic 36 is a *threshold* store 43 which stores a *threshold value* which indicates an amount of data of a frame that must be resident in the frame buffer 34 before transmission of that frame may be initiated by the transmit DMA logic and MAC 39." ('094; Col. 4: 32-37) (emphasis added). "When the *threshold amount* of data is resident in the buffer 34, then the transmit logic 39 is instructed to begin transmission of the frame. The transmit logic 39 then begins retrieving data from the buffer 34 to support transmission of the frame on the medium 42. This operation begins before the entire frame has been transferred from the host computer 30 into the buffer 34, if the transmit logic 39 is available to transmit the frame subject of the ongoing download from the host computer 30, the frame being downloaded into the buffer 34 is larger than the threshold set by the threshold store 43, and the host computer 30 indicates that immediate transmission of the data is desired." ('094; Col. 4: 59-Col. 5: 3)	some process to take place. DICTIONARY/TREATISE DEFINITIONS: threshold Webster's Ninth New Collegiate Dictionary (1983) Threshold - A level, point, or value above which something is true or will take place and below which it is not or will not. The American Heritage Dictionary of the English Language (4th ed. 2000) The point that must be exceeded to begin producing a given effect or result or to elicit a response. McGraw-Hill Electronics Dictionary (fifth edition, 1994) Threshold: 1. The least value of a current, voltage, or other quantity that produces the minimum detectable response. It is also called a limen. 2. The level of pumping at which a laser can go into self-excited oscillation. threshold value McGraw-Hill Electronics Dictionary (fifth edition, 1994) Threshold Value: The minimum input that produces a corrective action in an automatic control system. EXPERT TESTIMONY: Realtek's expert, Dr. Izhak Rubin, may provide testimony as to the

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	3Com reserves the right to rely on testimony by any expert in this action. See also U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and 6,570,884; Joint Claim Construction Statement in Cv-05-00098 (VRW). 3Com reserves the right to rely on any statement made by any party under the Patent Local Rules.	(emphasis added). "FIG. 1 illustrates a data communication system according to the present invention with a controller circuit using a dedicated transmit buffer memory which is automatically enabled to begin transmission of a frame on the network when the number of bytes available in the transmit buffer memory exceeds a preprogrammed *threshold*." ('094; Col. 3: 54-59) (emphasis added). "XMIT START THRESH provides for an early start of transmission. The XMIT START THRESH register is used to specify the number of transmit bytes that must reside on the adapter before it will start transmission. Values greater than the maximum frame length will prevent this function from operating properly. The method for disabling this function is to set the register to zero. Bytes are counted starting with the first byte of the destination field of the transmit frame. The number of bytes considered to be available is the sum of the immediate data written to XMIT AREA by the host and those bytes transferred to the transmit data buffers in the adapter using bus master DMA operations. The transmit request will be posted immediately after XMIT START THRESH transmit frame bytes are made available from the immediate data or when the adapter has bus-mastered XMIT START THRESH-XMIT IMMED LEN bytes	definition of the disputed terms as would be understood by one of ordinary skill in the relevant art and may provide an explanation of the technology.

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		onto the adapter. The number of bytes resident on the adapter must be equal to or greater than the value in XMIT START THRESH for the transmission to commence, unless the total frame size is less than XMIT START THRESH. In that case, the frame will begin transmission when the entire frame has been copied to the adapter. The actual transmission of the frame may be delayed by previous pending transmit frames and by deferrals to network traffic. This register is set to zero during a reset." ('094; Col. 20: 10-36) "The *threshold logic* determines the amount of immediate data from the descriptor, and monitors the downloading of data of the frame into the download area. When the combination meets the *threshold*, then actual transmission of the frame is initiated. Thus, transmission of a frame may be initiated before the complete frame has been downloaded into the download area." ('094; Col. 2: 40-46) (emphasis added). EXTRINSIC EVIDENCE: *DICTIONARY/TREATISE DEFINITIONS:* Webster's Ninth New Collegiate Dictionary (1983), pg.229: Threshold - "A level, point, or value above which something is true or will take place and below which it is not or will not."	

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*D-Link's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		EXPERT TESTIMONY: D-Link's expert, Howard Frazier, may provide testimony as to the definition of the disputed terms as would be understood by one of ordinary skill in the relevant art and may provide an explanation of the technology.	

4. U.S. Pat. No. 6,327,625

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
"**logic**" found in claim numbers: '625 patent: 23 also presented for construction in: '459 patent: 1 '872 patent: 1, 21 '884 patent: 1	PROPOSED CONSTRUCTION: Circuitry and/or programming DICTIONARY/TREATISE DEFINITIONS: See "**logic**" in subsection 1. INTRINSIC EVIDENCE: Claims: see, e.g., claim 2 ("2. The computer system of claim 1, comprising logic to maintain a list of packets stored in the buffer having the particular packet type, and wherein the logic to transfer packets is responsive to the list."); claim 3 ("3. The computer system of claim 1, comprising logic to set parameters associated with the packets in the buffer having the particular packet type, and the logic to transfer packets is responsive to the parameters."); claim 6 ("6. The computer system of claim 1, wherein the logic to transfer the packets includes processing resources which write a control field in the buffer in association with each packet, indicating the type of packet, whether the packet is ready for transfer, and whether the packet has already been transferred."; see also claim 1; claim 7; claim 8; claim 9; claim 10; claim 11; claim 12; claim 13; claim 23; claim 24; claim 25; claim 28; claim 29; claim 30; claim 31; claim 33; claim 34; claim 35; Specification: see, e.g., figs. 1, 3-8; col. 2:9-	Please refer to the construction under 35 U.S.C. § 112 ¶ 6 for the separate claim limitations of the identified claims. To the extent the term "logic" requires construction, Realtek asserts that "logic" (or "logic for") as used in the identified claims should be construed as "means" (or "means for") and, therefore, the associated claim elements should be governed by 35 U.S.C. § 112 ¶ 6. EXPERT TESTIMONY: Realtek's expert, Dr. Izhak Rubin and/or Dr. Nick Bambos, may provide testimony as to the definition of the disputed terms as would be understood by one of ordinary skill in the relevant art and may provide an explanation of the technology.

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	14 ("Logic is included in the network interface to transfer packets out of the buffer to the other of the first and second ports according to the order of receipt, and according to the respective packet types so that packets having a particular packet type are transferred out of the order of receipt relative to packets having other packet types."); col. 2:18-19 ("Logic maintains a list of packets stored in the buffer having a particular packet type."); col. 2:44-3:12 ("In yet another embodiment, the logic to transfer the packet includes processing resources which perform, in various combinations and orders, the following functions: set up a control field for each packet stored in the buffer in an order of receipt; write a parameter in the control field indicating the packet type has one of a plurality of packet types, including a first packet type, a second packet type and a third packet type; write a parameter in the control field indicating whether the packet has already been transferred; maintain a queue of entries identifying packets having the third packet type; process packets having the second packet type according to a particular process; write a parameter in the control field for packets having the second packet type indicating whether the packet is ready for transfer and the processing according to the particular process is complete; maintain an indicator of fullness of the buffer; transfer a packet from the buffer according to a priority rule which causes transfer of a packet identified by an entry in the queue ahead of packets in the buffer having the first and second packet types relative to the order of receipt, causes transfer of a packet having the first packet type in the order of receipt of the packet, if the parameters in the control field indicate the packet is ready for transfer, and the queue of entries is empty or the indicator of fullness exceeds a threshold, and skips transfer of a packet having the second packet type relative to the order of receipt if the parameter in the control field indicates the processing is not complete."); see also col. 2:19-21; col. 2:37-44; col. 3:18-20; col. 3:29-33; col. 3:51-52; col.	

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	3:61-67; col. 4:26-35; col. 4:39-40; col. 5:25-27; col. 5:55-57; col. 5:60-64; col. 6:5-11; col. 6:31-32; col. 6:42-45; col. 7:10-15; col. 8:1-6; col. 8:20-22; col. 8:28-30; col. 8:51-52; col. 8:61-64; col. 9:47-50; col. 9:57-59; col. 9:65-67; col. 10:3-5; col. 10:5-6; see also Prosecution History: Response to Office Action, May 1, 2001, p. 17-18; Response to Office Action, May 1, 2001, p. 18-19. EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action. See also U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and 6,570,884; Joint Claim Construction Statement in Cv-05-00098 (VRW). 3Com reserves the right to rely on any statement made by any party under the Patent Local Rules.	
"**logic to transfer packets out of the buffer**" found in claim numbers: '625 patent: 23	PROPOSED CONSTRUCTION: Circuitry and/or programming to transfer packets out of the buffer. DICTIONARY/TREATISE DEFINITIONS: See "**logic**" in subsection 1 for definitions of that term, "**frame transfer task**" in subsection 3 for definitions of "transfer," "**packet types**" in this section for definitions of "packet" and "**buffer**" in subsection 1. INTRINSIC EVIDENCE: Claims: see, e.g., claim 28 ("the logic to transfer the packets includes processing resources which write a control field in the buffer in association with each packet, indicating the type of packet, whether the packet is ready for transfer, and whether the packet has already been transferred"); see also claim 1; claim 2; claim 3; claim 6; claim 7; claim 8; claim 9; claim 10; claim 11; claim 12; claim 13; claim 23; claim 24; claim 25; claim 29; claim 30; claim 31;	PROPOSED CONSTRUCTION: device that transfers packets out of the buffer DICTIONARY/TREATISE DEFINITIONS: Synopsis, Inc., Electronic Design Automation Glossary of Terms The sequence of functions performed by hardware or software. Hardware logic is made up of circuits that perform an operation. Software logic is the sequence of instructions in a program. Newton's Telecom Dictionary: "**Logic**…a system that could be applied to the relationships between propositions to which only a binary choice of truth existed, i.e., yes or no." IBM Dictionary of Computing (10th ed. 1993): The systematized interconnection of digital switching functions, circuits, or devices.

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	claim 33; claim 34; claim 35; Specification: see, e.g., figs. 1, 3-8; col. 2:9-14 ("Logic is included in the network interface to transfer packets out of the buffer to the other of the first and second ports according to the order of receipt, and according to the respective packet types so that packets having a particular packet type are transferred out of the order of receipt relative to packets having other packet types"); see also col. 2:19-21; col. 2:37-3:12; col. 3:29-33; col. 3:61-67; col. 4:27-31; col. 8:4-9; col. 8:20-22; col. 8:28-30; col. 8:51-52; col. 8:61-64; col. 9:47-50; col. 9:57-59; col. 9:65-67; col. 10:3-5; see also Prosecution History: Response to Office Action, May 1, 2001, p. 17-18. EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action. See also U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and 6,570,884; Joint Claim Construction Statement in Cv-05-00098 (VRW). 3Com reserves the right to rely on any statement made by any party under the Patent Local Rules.	EXPERT TESTIMONY: Realtek's expert, Dr. Izhak Rubin, may provide testimony as to the definition of the disputed terms as would be understood by one of ordinary skill in the relevant art and may provide an explanation of the technology.
"**packet types**" found in claim numbers: '625 patent: 23	PROPOSED CONSTRUCTION: Packets with different formats and priorities DICTIONARY/TREATISE DEFINITIONS: packet type: Newton's Telecom Dictionary (17th ed. 2001): Packet type identifier: In packet data networking technology, the third octet in the packet header that identifies the packet's function and, if applicable, its sequence number. INTRINSIC EVIDENCE: Claims: see, e.g., claim 14 ("The computer system of claim 13, wherein the particular type of packet comprises a priority packet, and the second type of packet comprises a packet suitable for processing with a	PROPOSED CONSTRUCTION: Packets with different formats or priorities. DICTIONARY/TREATISE DEFINITIONS: Webster's New World Dictionary (1991) "**type … 4** a kind, class, or group having distinguishing characteristics in common…." INTRINSIC EVIDENCE: '625 patent, claim 26 ("The integrated circuit of claim 23, wherein *the particular type of packet comprises a priority packet*.")

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	security protocol."); see also claim 1; claim 2; claim 3; claim 7; claim 8; claim 9; claim 10; claim 11; claim 12; claim 13; claim 15; claim 18; claim 19; claim 21; claim 22; claim 23; claim 24; claim 25; claim 26; claim 27; claim 29; claim 30; claim 31; claim 33; claim 34; claim 35; Specification: see, e.g., Figs. 2, 3 ("FIG. 3 is a diagram illustrating the function of the packet filter in the system of FIG. 1."); col. 2:44-3:12 ("In yet another embodiment, the logic to transfer the packet includes processing resources which perform, in various combinations and orders, the following functions: set up a control field for each packet stored in the buffer in an order of receipt; write a parameter in the control field indicating the packet type has one of a plurality of packet types, including a first packet type, a second packet type and a third packet type; write a parameter in the control field indicating whether the packet has already been transferred; maintain a queue of entries identifying packets having the third packet type; process packets having the second packet type according to a particular process; write a parameter in the control field for packets having the second packet type indicating whether the packet is ready for transfer and the processing according to the particular process is complete; maintain an indicator of fullness of the buffer; transfer a packet from the buffer according to a priority rule which causes transfer of a packet identified by an entry in the queue ahead of packets in the buffer having the first and second packet types relative to the order of receipt, causes transfer of a packet having the first packet type in the order of receipt of the packet, if the parameters in the control field indicate the packet is ready for transfer, and the queue of entries is empty or the indicator of fullness exceeds a threshold, and skips transfer of a packet having the second packet type relative to the order of receipt if the parameter in the control field indicates the processing is not complete."); see also col. 1:58-61; col. 2:5-9; col. 2:15-3:12; col. 4:11-13; col. 5:6-7; col. 5:17-21; see also Prosecution History: Office Action,	'625 patent, claim 27 ("The integrated circuit of claim 23, wherein *the particular type of packet comprises a packet suitable for processing with a security protocol*."). '625 patent at 2:15-44 ("In one embodiment, a data filter is coupled with the buffer to generate identifiers identifying packets of data stored in the buffer as members of one of a plurality of packet types. *Logic maintains a list of packets stored in the buffer having a particular packet type*. The logic to transfer the packets is responsive to the list to determine the order in which a given packet is transferred out of the buffer. *Thus for example, priority packets are identified* and entries placed in a queue of priority packets on the network interface. … In another embodiment, *packets of the particular types are suitable for processing* according to a process such as an encryption or authentication process.") '625 patent at 5:17-21 ("In this embodiment, *the packet filter identifies three classes of packets*. The first type of packet is *normal* packet is indicated by branch 103. Second type of packet is the *IPsec* packet is the indicated by branch 104. The third type of packet is the *priority* packet as indicated by branch 105.") '625 patent, at 1:23-41 ("As computer networks are adapted to carry a variety of types of traffic, *network protocols are being developed to support variant processing of packets as they traverse the network*. Thus, *priority packets* are developed which are suitable for carrying real-time video or audio signals. …. Also, *network security is supported for some types of packets*. Thus, the Internet security IPsec protocols are being developed.") '625 patent, at 1:58-61 ("The present invention *provides support for priority and Internet Protocol security packets*, and other protocols at the network interface level and in conjunction with FIFO-based packet buffers.") '625 patent, Abstract ("*Support for priority*

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	Feb. 2, 2001, pp. 3-4; Response to Office Action, May 1, 2001, p. 17-18; Response to Office Action, May 1, 2001, p. 18-19; Response to Office Action, May 1, 2001, p. 20. EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action. See also U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and 6,570,884; Joint Claim Construction Statement in Cv-05-00098 (VRW). 3Com reserves the right to rely on any statement made by any party under the Patent Local Rules.	*and IP security packets, and other protocols at the network interface level* and in conjunction with FIFO-based packet buffers is provided by allowing out of order processing of certain packets in the FIFO. . . . Logic is included in the network interface to transfer packets out of the buffer according to the order of receipt, and according to the respective packet types so that packets having a particular packet type are transferred out of the order of receipt relative to packets having other packet types.") DICTIONARY/TREATISE DEFINITIONS: EXPERT TESTIMONY: Realtek's expert, Dr. Nick Bambos, may provide testimony as to the definition of the disputed terms as would be understood by one of ordinary skill in the relevant art and may provide an explanation of the technology.

5. U.S. Pat. No. 6,526,446

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
"**data download circuit**" found in claim numbers: '446 patent: 26	PROPOSED CONSTRUCTION: A circuit that retrieves data from memory DICTIONARY/TREATISE DEFINITIONS: See "**data value**" in subsection 6 for definitions of "data;" download: The American Heritage Dictionary of the English Language (4th ed. 2000): To transfer (data or programs) from a server or host computer to one's own computer or device; circuit: The American Heritage Dictionary of the English Language (4th ed. 2000): The combination of a number of electrical devices and conductors that, when interconnected to a form a conducting path, fulfill some desired function; see also Dictionary of Computing (1st ed. 1983): Circuit: 1. The combination of a number of electrical devices and conductors that, when interconnected to form a conducting path, fulfill some desired function. 2. A physical (electrical) connection used for	PROPOSED CONSTRUCTION: The circuitry that downloads data corresponding to the frame segment descriptor. INTRINSIC EVIDENCE: '446 patent at 8:28-38 ("With reference still to FIG. 2, *data download DMA circuit 212 utilizes the descriptors to retrieve and download the data file*, TCP templates, IP templates, and frame header stored within host memory 106. . . . *In other words, data download DMA circuit 212 receives the descriptor information from hardware queue 210 and uses it to retrieve the actual data stored within host memory 106.*") '446 patent, Abstract ("Hardware only transmission control protocol segmentation for a high performance network interface card. Specifically, one embodiment of the present invention includes a circuit for

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	communication. Dictionary of Computing (3d ed. 1990): Circuit: The combination of a number of electrical devices and conductors that, when interconnected to form a conducting path, fulfill some desired function. INTRINSIC EVIDENCE: Claims: see, e.g., claim 1 ("A circuit for implementing transmission control protocol segmentation, said circuit comprising: a segmentation circuit coupled to receive a descriptor from a host device which corresponds to data, said segmentation circuit utilizes said descriptor to generate a frame segment descriptor; a data download circuit coupled to said segmentation circuit to receive said frame segment descriptor, said data download circuit retrieves said data from a memory; and a medium access control circuit coupled to said data download circuit to receive said data in a frame segment."); claim 14 ("said data download circuit comprises a data download direct memory access circuit"); see also claim 4; claim 8; claim 15; claim 16; claim 18; claim 25; claim 26; Specification: Fig. 2; Fig. 4; col. 2:29-34; col. 2:52-57; col. 2:54-67; 8:28-38. EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action. See also U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and 6,570,884; Joint Claim Construction Statement in Cv-05-00098 (VRW). 3Com reserves the right to rely on any statement made by any party under the Patent Local Rules.	implementing transmission control protocol (TCP) segmentation. The circuit includes a segmentation circuit coupled to receive a descriptor from a host device which corresponds to data. *The segmentation circuit utilizes the descriptor to generate other descriptors that describe each frame segment. Furthermore, the circuit also includes a data download circuit coupled to the segmentation circuit to receive the frame segment descriptors. Specifically, the data download circuit retrieves the data from a memory.* Moreover, *the circuit includes a medium access control circuit coupled to the data download circuit to receive the data in a frame segment*.") '446 patent, Fig. 2 (showing Host Driver 202, Descriptor DMA 204, Segmentation State Machine 208, Hardware Queue 210, Data Download DMA 212, etc.) '446 patent, Fig. 4 ("receiving from a host device a descriptor signal corresponding to data stored within memory; *using the descriptor signal to generate a frame segment descriptor; receiving the data from the memory using a data download circuit*, etc.) DICTIONARY/TREATISE DEFINITIONS: circuit Newton's Telecom Dictionary (eleventh ed., 1996) Circuit: The physical connection (or path) of channels, conductors and equipment between two given points through which an electric current may be established. Includes both sending and receiving capabilities. A circuit can also be a network of circuit elements, such as resistors, inductors, capacitors, semiconductors, etc., that performs a specific function. A circuit can also be a closed path through which current can flow. The American Heritage Dictionary of the English Language (4th ed. 2000) The combination of a number of electrical devices and conductors that, when interconnected to a form a conducting path, fulfill some desired function.

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		download The American Heritage Dictionary of the English Language (4th ed. 2000) To transfer (data or programs) from a server or host computer to one's own computer or device. EXPERT TESTIMONY: Realtek's expert, Dr. Nick Bambos, may provide testimony as to the definition of the disputed terms as would be understood by one of ordinary skill in the relevant art and may provide an explanation of the technology.
"**descriptor signal**" found in claim numbers: '446 patent: 26	PROPOSED CONSTRUCTION: A signal that describes data. DICTIONARY/TREATISE DEFINITIONS: See "**descriptor**" in this subsection and "**indication signal**" in subsection 1 for definitions of "signal." INTRINSIC EVIDENCE: Claims: claim 26; claim 30; claim 31; claim 32; claim 33; Specification: see, e.g., figs. 2-5; col. 2:43-46 ("the circuit includes a retriever circuit coupled to receive the first signal from the host device which indicates where a descriptor is located within the host memory. The retriever circuit also retrieves the descriptor which describes data stored within the host memory."); see also Fig. 4; col. 2:60-65; col. 3:23-26; col. 5:66-6:6; col. 6:19-22; col. 10:41-46; col. 11:1-4. EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action. See also U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and 6,570,884; Joint Claim Construction Statement in Cv-05-00098 (VRW). 3Com reserves the right to rely on any statement made by any party under the	PROPOSED CONSTRUCTION: A signal indicating where the corresponding data is in the host memory. INTRINSIC EVIDENCE: '446 patent at 5:66-6:6 ("Referring to FIG. 2, *a host driver 202* running on processor 106 of host system 100 *is responsible for creating a descriptor for a data file stored within host memory* 106 which is to be eventually transferred by network interface card (NIC) 118 over network 120. *The descriptor includes information about where the data file is stored within host memory 106*, the size of the data file, along with other information.") '446 patent at 6:19-22 ("*More specifically, the descriptor structure prepared by host driver 202 consists of* control words, *fragment address*, and fragment length. The control words contain packet related information and flags.") '446 patent, Abstract ("Hardware only transmission control protocol segmentation for a high performance network interface card. . . . The circuit includes a segmentation circuit coupled *to receive a descriptor from a host device which corresponds to data.* The segmentation circuit utilizes the descriptor to generate other descriptors that describe each frame segment. . . .") Fig. 4 (showing separate steps, including "receiving from a host device *a descriptor*

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	Patent Local Rules.	*signal corresponding to data stored within memory*") DICTIONARY/TREATISE DEFINITIONS: Dictionary of Computing (3d ed. 1990): Stored information that describes how other information is stored, e.g. in an array, record, or file. By referring to the descriptor, a program can interpret the other data. The American Heritage Dictionary of the English Language (4th edition, 2000) A word, phrase, or alphanumeric character used to identify an item in an information storage and retrieval system. IBM Dictionary of Computing (10th ed. 1993): A word or phrase used to categorize or index information. EXPERT TESTIMONY: Realtek's expert, Dr. Nick Bambos, may provide testimony as to the definition of the disputed terms as would be understood by one of ordinary skill in the relevant art and may provide an explanation of the technology.
"**a descriptor signal which corresponds to data stored within memory**" found in claim numbers: '446 patent: 26	PROPOSED CONSTRUCTION: The descriptor signal describes data stored within host memory. DICTIONARY/TREATISE DEFINITIONS: See "**descriptor**" in this subsection for definitions of that term, "**indication signal**" in subsection 1 for definitions of "signal," "**data value**" in subsection 6 for definitions of "data" and "**buffer memory**" in subsection 1 for definitions of "memory"; correspond: The American Heritage Dictionary of the English Language (4th ed. 2000): To be in agreement, harmony, or conformity. To be similar or equivalent in character, quantity, origin, structure, or function: English navel corresponds to Greek omphalos. See Synonyms at agree. To communicate by letter, usually over a period of time.	

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	INTRINSIC EVIDENCE: Claims: claim 1; claim 26; Specification: see, e.g., figs. 2-5; col. 2:43-46 ("the circuit includes a retriever circuit coupled to receive the first signal from the host device which indicates where a descriptor is located within the host memory. The retriever circuit also retrieves the descriptor which describes data stored within the host memory."); see also col. 2:25-27; col. 2:60-62; col. 6:51-55; col. 10:40-42. EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action. See also U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and 6,570,884; Joint Claim Construction Statement in Cv-05-00098 (VRW). 3Com reserves the right to rely on any statement made by any party under the Patent Local Rules.	
"**frame segment descriptor**" found in claim numbers: '446 patent: 26	PROPOSED CONSTRUCTION: A descriptor for a frame segment. INTRINSIC EVIDENCE: Claims: claim 1; claim 15; claim 26; claim 31; claim 32; claim 33; Specification: figs. 2-5; col. 2:29-31 ("the segmentation circuit utilizes the descriptor to generate other descriptors that describe each frame segment."); Fig. 4; col. 2:27-37; col. 2:50-54; col. 2:63-65; col. 3:23-26; col. 6:58-7:14; col. 10:44-57; col. 11:1-4. EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action. See also U.S. Patent Nos. 5,434,872;	PROPOSED CONSTRUCTION: A descriptor identifying where the corresponding frame segment is in the host memory. INTRINSIC EVIDENCE: '446 patent at 6:58-7:14 ("Conversely, if the data file needs TCP segmentation, *TCP segmentation state machine 208 creates another set of descriptors wherein each descriptor describes a fragment or a segment of the data file*. In other words, the data file stored within host memory 106 is virtually segmented down into a number of *frames. Within the present embodiment, each of the descriptors created by TCP segmentation state machine 208 is going to contain a pointer to a location in host memory 106* where a reusable "template" for the IP header is stored. Furthermore, each descriptors is also going to contain a pointer to a location in host memory 106 where a reusable "template" for the TCP header is stored. *Additionally, each of the*

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	5,732,094; 6,327,625; 6,526,446; and 6,570,884; Joint Claim Construction Statement in Cv-05-00098 (VRW). 3Com reserves the right to rely on any statement made by any party under the Patent Local Rules.	*descriptors would also include* a control word along with *pointers to where the data file (payload) is stored within host memory 106*. Also, each descriptor *contains a pointer to a location in host memory 106 where a reusable template* for the Medium Access Control (MAC) header *is stored.* These descriptors are then transmitted by TCP segmentation state machine 208 to hardware queue 210 for temporary storage. . . . As such, TCP segmentation state machine 208 transmits the revised structure descriptors to hardware queue 210 where they are temporarily stored. *This revised structure descriptor information stored within hardware queue 210 will subsequently be used by data download DMA circuit 212 to transfer data.*") '446 patent, Abstract ("Hardware only transmission control protocol segmentation for a high performance network interface card. Specifically, one embodiment of the present invention includes a circuit for implementing transmission control protocol (TCP) segmentation. The circuit includes a segmentation circuit coupled to receive a descriptor from a host device which corresponds to data. *The segmentation circuit utilizes the descriptor to generate other descriptors that describe each frame segment. Furthermore, the circuit also includes a data download circuit coupled to the segmentation circuit to receive the frame segment descriptors*. Specifically, the data download circuit retrieves the data from a memory. Moreover, the circuit includes a medium access control circuit coupled to the data download circuit *to receive the data in a frame segment.* ") '446 patent, Fig. 4 ("receiving from a host device a descriptor signal corresponding to data stored within memory; *using the descriptor signal to generate a frame segment descriptor; receiving the data from the memory using a data download circuit*, etc.) '446 patent at 2: 27-37 ("The circuit includes a segmentation circuit coupled to

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		receive a descriptor from a host device which corresponds to data. *The segmentation circuit utilizes the descriptor to generate other descriptors that describe each frame segment.* Furthermore, the circuit also includes *a data download circuit coupled to the segmentation circuit to receive the frame segment descriptors.* Specifically, the data download circuit retrieves the data from a memory. Moreover, the circuit includes a medium access control circuit coupled to the data download circuit *to receive the data in a frame segment.*") EXPERT TESTIMONY: Realtek's expert, Dr. Nick Bambos, may provide testimony as to the definition of the disputed terms as would be understood by one of ordinary skill in the relevant art and may provide an explanation of the technology.

6. U.S. Pat. No. 6,570,884

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
"**data value**" found in claim numbers: '884 patent: 1	PROPOSED CONSTRUCTION: A value of bit(s) of data. DICTIONARY/TREATISE DEFINITIONS: data: Dictionary of Computing (1st ed. 1983): Information that has been prepared, often in a particular format, for a specific purpose; see also Microsoft Computer Dictionary (5th ed. 2002): Plural of the Latin datum, meaning an item of information; Dictionary of Computing (3d ed. 1990): Information that has been prepared, often in a particularly format, for a specific purpose; Webster's New World Computer Dictionary (10th ed. 2003): Factual information (such as text, numbers, sounds, and images) in a form that can be processed by a computer. McGraw-Hill Illustrated Telecom Dictionary (2d ed. 2000): In the communications industry, data is anything that is transmitted or processed digitally. INTRINSIC EVIDENCE:	Realtek has asserted that claim 1 of the '884 patent is invalid under 35 U.S.C. § 112 ¶ 1 or 2, because it is unclear what the claimed "data value" is and the '884 patent specification fails to provide any written description, support, or definition of the term. In the event that the Court decides to construe the term, Realtek asserts that it should be construed as "one of a discard command for discarding packets and a continue command for letting packets continue to the host." INTRINSIC EVIDENCE: '884 patent at 10:30-35 ("When the ARM7 is done processing the data, *it can flush the packet from the FIFO by issuing either an discard command or an continue command via the Command register.* The former command discards the packet while the latter command lets the packet continue to the host.")

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	Claims: claim 1; claim 21; Specification: see, e.g., figs. 1, 3, 5; col. 10:31-35 ("When the ARM7 is done processing the data, it can flush the packet from the FIFO by issuing either an discard command or an continue command via the Command register."); col. 10:49-53 ("the processor may pull out data such as IP addresses or other data used at the interface, or the processor may initiate an action such as re-boot or power up of the host processor, or resetting the interface card"); see also col. 9:10-15; col. 9:24-26; col. 10:33-34; col. 10:61-65; see also Prosecution History: RCE and Amendment, Aug. 15, 2002, p. 7; RCE and Amendment, Aug. 15, 2002, p. 11; Response to Office Action, Jan. 22, 2003, p. 8; Notice of Allowance, Feb. 2, 2003, p. 2. EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action. See also U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and 6,570,884; Joint Claim Construction Statement in Cv-05-00098 (VRW). 3Com reserves the right to rely on any statement made by any party under the Patent Local Rules.	'884 File History, Bates No. 3COM11743 (Rule 1.121 Marked-Up Claims), lines 11-13 ("second logic coupled with the buffer, and responsive to the packet filter to read and process data in the identified packets from the buffer, and to produce *a data value dependent on contents of the packet* prior to transfer of the identified packets to the second port but the first logic.")(underline text added to the claim during the prosecution of the '884 patent.) DICTIONARY/TREATISE DEFINITIONS: data: Dictionary of Computing (3d ed. 1990) Information that has been prepared, often in a particularly format, for a specific purpose Microsoft Computer Dictionary (5th ed. 2002) Plural of the Latin datum, meaning an item of information Webster's New World Computer Dictionary (10th ed. 2003): Factual information (such as text, numbers, sounds, and images) in a form that can be processed by a computer. EXPERT TESTIMONY: Realtek's expert, Dr. Nick Bambos, may provide testimony as to the definition of the disputed terms as would be understood by one of ordinary skill in the relevant art and may provide an explanation of the technology.
"**first logic**" found in claim numbers: '884 patent: 1	PROPOSED CONSTRUCTION: First Circuitry and/or programming. DICTIONARY/TREATISE DEFINITIONS: See "**logic**" in subsection 1. INTRINSIC EVIDENCE: See "**logic**" in this section. EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field	Please refer to the construction under 35 U.S.C. § 112 ¶ 6 identified below. To the extent this term requires construction, Realtek asserts that "logic" should be construed as "means" (or "means for") and, therefore, this claim element should be governed by 35 U.S.C. § 112 ¶ 6. If the Court determines that 35 U.S.C. § 112 ¶ 6 does not apply, "first logic" should be construed as "first device." DICTIONARY/TREATISE DEFINITIONS: Synopsis, Inc., Electronic Design Automation Glossary of Terms

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action. See also U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and 6,570,884; Joint Claim Construction Statement in Cv-05-00098 (VRW). 3Com reserves the right to rely on any statement made by any party under the Patent Local Rules.	The sequence of functions performed by hardware or software. Hardware logic is made up of circuits that perform an operation. Software logic is the sequence of instructions in a program. Newton's Telecom Dictionary: "**Logic**…a system that could be applied to the relationships between propositions to which only a binary choice of truth existed, i.e., yes or no." IBM Dictionary of Computing (10th ed. 1993): The systematized interconnection of digital switching functions, circuits, or devices. EXPERT TESTIMONY: Realtek's expert, Dr. Nick Bambos, may provide testimony as to the definition of the disputed terms as would be understood by one of ordinary skill in the relevant art and may provide an explanation of the technology.
"**host system**" found in claim numbers: '884 patent: 1	PROPOSED CONSTRUCTION: A computer that communicates over a network. DICTIONARY/TREATISE DEFINITIONS: Webster's New World Computer Dictionary (10th ed. 2003): 1. In the Internet, any computer that can function as the beginning and end point of data transfers. An Internet host has a unique Internet address (called an IP address) and a unique domain name; Dictionary of Computing (3d ed. 1990): Host computer (host): A computer that is attached to a network and provides services other than simply acting as a store-and-forward processor or communication switch. INTRINSIC EVIDENCE: Claims: see, e.g., claim 1; claim 11; claim 12; claim 15; claim 16; claim 20; claim 21; claim 29; claim 30; claim 39; claim 40; claim 44; claim 45; Specification: see, e.g., col. 1:28-33 ("The NIC Device-Class Power Management Specification handles the situation in which a host processor running Windows or another operating	PROPOSED CONSTRUCTION: Any system or computer that communicates over a network Evidence (872: Col 1: lns. 65-67) (094: Col. 1, lns. 60-62) Furthermore, the prior art systems which use transmit data buffers require the *host or sending system* to manage the transmit data buffer. (872: Col. 3, ln. 65 to col. 4., ln. 2) ('094: Col. 3, lns. 59-64) As shown in FIG. 1, such system for communicating data includes a host data processing system, generally referred to by reference number 1, which includes a host system bus 2, a host central processing unit 3, host memory 4, and other host devices 5, all communicating across the bus 2 (884: Col. 2, lns. 39-44) The invention is particularly suited to environments in which the host system is actively handling communications and other processing tasks,

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	system OS wants to go to sleep, yet allow others to access any shared directories or devices it might have offered to the network."); col. 2:27-29 ("In another embodiment the intercept technique of the present invention is used for tracking the host computer's IP address."); see also col. 1:8-11; col. 1:18-25; col. 1:33-38; col. 1:66-2:5; col. 2:20-26; col. 2:29-45; col. 3:19-22; col. 3:34-35; col. 4:11-13; col. 4:18-24; col. 4:46-51; col. 4:59-60; col. 5:39-41; col. 7:2-5; col. 7:29-33; col. 9:6-15; col. 9:24-27; col. 10:33-34; col. 10:49-53; col. 1:16-17; col. 2:40-44; col. 4:37-51;10:53-58; see also Prosecution History: Office Action, p. 5; Office Action, p. 6; Response to Office Action, May 14, 2001, p. 6; Office Action, Jul. 26, 2001, p. 4; Office Action, Jul. 26, 2001, p. 6; Response to Office Action, Oct. 26, 2001, p. 2; Final Office Action, Mar. 20, 2002, p. 4; Final Office Action, Mar. 20, 2002, p. 6; RCE and Amendment, Aug. 15, 2002, p. 7; RCE and Amendment, Aug. 15, 2002, p. 8; RCE and Amendment, Aug. 15, 2002, p. 10; RCE and Amendment, Aug. 15, 2002, p. 11; RCE and Amendment, Aug. 15, 2002, p. 12; Office Action, Nov. 4, 2002, p. 6; Office Action, Nov. 4, 2002, p. 8; Response to Office Action, Jan. 22, 2003, p. 8; Response to Office Action, Jan. 22, 2003, p. 9; Response to Office Action, Jan. 22, 2003, p. 11; Response to Office Action, Jan. 22, 2003, p. 13-14; Response to Office Action, Jan. 22, 2003, p. 15; Notice of Allowance, Feb. 2, 2003, p. 2. EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael Mitzenmacher, may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on any testimony given by any of the other experts in this action. See also U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and 6,570,884; Joint Claim Construction	and in which the adapter is able to take over some specialized tasks without interfering with the active processing in the host system.

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	Statement in Cv-05-00098 (VRW). 3Com reserves the right to rely on any position taken by the parties under the Patent Local Rules.	
"**logic**" found in claim numbers: '884 patent: 1 also presented for construction in: '459 patent: 1 '872 patent: 1, 21 '625 patent: 23	PROPOSED CONSTRUCTION: Circuitry and/or programming DICTIONARY/TREATISE DEFINITIONS: See "**logic**" in subsection 1. INTRINSIC EVIDENCE: Claims: see, e.g., claim 2 ("2. The interface of claim 1, wherein the second logic comprises a general purpose processor module."); claim 7 ("7. The interface of claim 2, wherein the first port, buffer, second port, packet filter, first logic and processor comprise components of a single integrated circuit."); claim 11 ("11. The interface of claim 1, wherein the second logic to process the packet comprises a routine to discover an internet protocol IP address of the host system."); claim 12 ("12. The interface of claim 1, wherein the second logic to process the packet comprises a routine to issue a reboot command to the host system."); see also claim 1; claim 8; claim 9; claim 10; claim 13; claim 14; claim 15; claim 16; claim 17; claim 18; claim 19; claim 20; claim 28; claim 31; claim 32; claim 33; claim 34; claim 37; claim 38; claim 39; claim 40; claim 41; claim 46; Specification: see, e.g., figs. 1-5; col. 1:61-66 ("The present invention provides a network interface card, or an interface to other types of communication channels, with limited intelligence, implemented using a relatively slower, and lower cost embedded processor, supported by dedicated hardware logic for the purposes of intercepting certain packets being received via the network."); col. 2:51-52 ("According to various aspects of the invention, the packet filter comprises one or more match logic circuits."); see also col. 2:13-16; col. 2:52-53; col. 2:55-59; col. 2:65-3:10; col. 3:13-22; col. 3:35-39; col. 3:41-43; col. 3:48-56; col. 3:65-67; col. 4:1-4; col. 4:16-17; col. 4:57-60; col. 4:63-65; col. 5:3-7; col. 5:37-38; col. 5:43-	Please refer to the construction under 35 U.S.C. § 112 ¶ 6 for the separate claim limitations of separate claims. To the extent this term requires construction, Realtek asserts that "logic" (or "logic for") should be construed as "means" (or "means for") and, therefore, the associated claim elements should be governed by 35 U.S.C. § 112 ¶ 6. If the Court determines that 35 U.S.C. § 112 ¶ 6 does not apply, "logic" should be construed as "device." DICTIONARY/TREATISE DEFINITIONS: Synopsis, Inc., Electronic Design Automation Glossary of Terms The sequence of functions performed by hardware or software. Hardware logic is made up of circuits that perform an operation. Software logic is the sequence of instructions in a program. Newton's Telecom Dictionary: "**Logic**…a system that could be applied to the relationships between propositions to which only a binary choice of truth existed, i.e., yes or no." IBM Dictionary of Computing (10th ed. 1993): The systematized interconnection of digital switching functions, circuits, or devices. EXPERT TESTIMONY: Realtek's expert, Dr. Nick Bambos, may provide testimony as to the definition of the disputed terms as would be understood by one of ordinary skill in the relevant art and may provide an explanation of the technology.

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	46; col. 5:50-6:7; col. 6:13-15; col. 6:21-24; col. 6:26-31; col. 6:33-35; col. 6:49-50; col. 6:62-63; col. 8:57-62; col. 10:3-5; col. 10:61-65; see also Prosecution History: Office Action, p. 3; Office Action, p. 4; Response to Office Action, May 14, 2001, p. 2; Response to Office Action, May 14, 2001, p. 3; Response to Office Action, May 14, 2001, p. 6; Office Action, Jul. 26, 2001, p. 3; Office Action, Jul. 26, 2001, p. 5; Response to Office Action, Oct. 26, 2001, p. 2; Response to Office Action, Oct. 26, 2001, p. 3; Final Office Action, Mar. 20, 2002, p. 3; Final Office Action, Mar. 20, 2002, p. 5; Final Office Action, Mar. 20, 2002, p. 7; Final Office Action, Mar. 20, 2002, p. 8; RCE and Amendment, Aug. 15, 2002, p. 7; RCE and Amendment, Aug. 15, 2002, p. 8; RCE and Amendment, Aug. 15, 2002, p. 10; RCE and Amendment, Aug. 15, 2002, p. 11; RCE and Amendment, Aug. 15, 2002, p. 12; Office Action, Nov. 4, 2002, pp. 4-5; Office Action, Nov. 4, 2002, p. 7; Response to Office Action, Jan. 22, 2003, p. 8; Response to Office Action, Jan. 22, 2003, p. 9; Response to Office Action, Jan. 22, 2003, p. 11; Response to Office Action, Jan. 22, 2003, p. 12; Response to Office Action, Jan. 22, 2003, p. 13; Response to Office Action, Jan. 22, 2003, p. 14; Response to Office Action, Jan. 22, 2003, p. 15; Notice of Allowance, Feb. 2, 2003, p. 2. EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action. See also U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and 6,570,884; Joint Claim Construction Statement in Cv-05-00098 (VRW). 3Com reserves the right to rely on any	

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	statement made by any party under the Patent Local Rules.	
"**read and process data in the identified packets from the buffer**" found in claim numbers: '884 patent: 1	PROPOSED CONSTRUCTION: read and process data in the identified packets from the buffer INTRINSIC EVIDENCE: Claims: see, e.g., claim 37 ("logic which signals the processor to process the data after at least part of the identified packet is stored in the buffer"); claim 38 ("logic which signals the processor to process the data after the identified packet is stored in the buffer"); see also claim 1; claim 21; claim 40; Specification: figs. 1-5; col. 6:38-40 ("In an alternative embodiment, the packet is supplied in parallel to a RAM buffer which is independent of the receive FIFO"); Fig. 5; 6:36-37; 3:19-26; 6:58-7:7; see also Prosecution History: RCE and Amendment, Aug. 15, 2002, p. 7; RCE and Amendment, Aug. 15, 2002, p. 11; RCE and Amendment, Aug. 15, 2002, p. 12; Response to Office Action, Jan. 22, 2003, p. 8; Response to Office Action, Jan. 22, 2003, p. 13-14; Notice of Allowance, Feb. 2, 2003, p. 2. EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action. See also U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and 6,570,884; Joint Claim Construction Statement in Cv-05-00098 (VRW). 3Com reserves the right to rely on any statement made by any party under the Patent Local Rules.	PROPOSED CONSTRUCTION: read and process data in the identified packets while the packets are in the buffer INTRINSIC EVIDENCE: '884 patent at 6:36-37 ("*The processor accesses the packet from the receive FIFO 201 for processing.*") '884 File History, Bates No. 3COM11713, lines 6-8 ("The present invention is directed to a network interface which *has logic to process packets in the frame buffer* that are identified by a packet filter as having a particular format, *before the packets are transferred* to the host processor to which they are addressed.") '884 patent at 3:19-26 ("When a particular packet in the FIFO buffer reaches a stage for upload to the host computer, the logic on the network interface card issues an interrupt to the processor on the network interface card if a flag is set. *In response to the interrupt, the packet in the FIFO buffer is processed locally on the network interface card.* If the FIFO buffer overflows during the processing of the packet, then packets may be lost.") '884 patent at 6:58-7:7 ("FIG. 5 illustrates the processing which occurs upon interrupting the processor, and the handling of the packet by the processor. *The process begins when a packet is at the top of the receive FIFO* by testing the packet header (block 400). The logic determines whether a pattern match bit is set (block 41). *If the pattern match bit is set, then the processor is interrupted and the receive FIFO is stalled (block 402).* . . . Upon receiving the interrupt, the processor handles the packet (block 403). . . . Upon completion of processing, *the FIFO is "un-stalled" to begin continued handling of the data flow (block 405).*") '884 File History, Bates No. 3COM11743 (Rule 1.121 Marked-Up Claims), lines 11-13 ("second logic coupled with the buffer, and

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		responsive to the packet filter *to read and process data in the identified packets from the buffer*, and to produce a data value dependent on contents of the packet prior to transfer of the identified packets to the second port but the first logic.") (underline text added to the claim during the prosecution of the '884 patent.) '884 patent, Fig. 5 ("402 INTERRUPT PROCESSOR/STALL FIFO; 403 PROCESS PACKET; 404 DISCARD PARKET [sic], MODIFY PACKET, OR DO NOTHING TO PACKET; 404 "UN-STALL" FIFO"; 406 PROCEED) EXPERT TESTIMONY: Realtek's expert, Dr. Nick Bambos, may provide testimony as to the definition of the disputed terms as would be understood by one of ordinary skill in the relevant art and may provide an explanation of the technology.
"**second logic**" found in claim numbers: '884 patent: 1	PROPOSED CONSTRUCTION: Second Circuitry and/or programming DICTIONARY/TREATISE DEFINITIONS: See "**logic**" in subsection 1. INTRINSIC EVIDENCE: See "**logic**" in this section. EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action. See also U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and 6,570,884; Joint Claim Construction Statement in Cv-05-00098 (VRW). 3Com reserves the right to rely on any statement made by any party under the Patent Local Rules.	Please refer to the construction under 35 U.S.C. § 112 ¶ 6 identified below. To the extent this term requires construction, Realtek asserts that "logic" should be construed as "means" and, therefore, this claim element should be governed by 35 U.S.C. § 112 ¶ 6. If the Court determines that 35 U.S.C. § 112 ¶ 6 does not apply, "second logic" should be construed as "second device." DICTIONARY/TREATISE DEFINITIONS: Synopsis, Inc., Electronic Design Automation Glossary of Terms The sequence of functions performed by hardware or software. Hardware logic is made up of circuits that perform an operation. Software logic is the sequence of instructions in a program. Newton's Telecom Dictionary: "**Logic**…a system that could be applied to the relationships between propositions to which only a binary choice of truth existed, i.e., yes or no." IBM Dictionary of Computing (10th ed.

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
		1993): The systematized interconnection of digital switching functions, circuits, or devices. EXPERT TESTIMONY: Realtek's expert, Dr. Nick Bambos, may provide testimony as to the definition of the disputed terms as would be understood by one of ordinary skill in the relevant art and may provide an explanation of the technology.
"**variant formats**" found in claim numbers: '884 patent: 1	PROPOSED CONSTRUCTION: Varying arrangements of packet information other than a destination MAC address DICTIONARY/TREATISE DEFINITIONS: variant: The American Heritage Dictionary of the English Language (4th ed. 2000): Having or exhibiting variation; differing. INTRINSIC EVIDENCE: Claims: see, e.g., claim 9 ("the packet filter comprises: mask logic circuits, having a mask and a mask modifier logic to modify the mask using the mask modifier in response to the packet; hash logic to generate a hash in response to the packet and the mask; and compare logic to compare the hash generated with an expected hash for one of the plurality of variant formats."); see also claim 1; claim 8; claim 10; claim 16; claim 17; claim 18; claim 19; claim 20; claim 21; claim 31; claim 32; claim 33; claim 34; claim 40; claim 41; claim 46; Specification: see, e.g., figs. 4, 5; col. 2:52-53 ("The match logic circuits comprise mask logic circuits that store a mask identifying selected bytes within a packet of a particular format in the plurality of variant formats."); see also col. 2:5-7; col. 3:16-19; col. 3:39-41; col. 3:48-52; col. 4:24-26; col. 5:3-5; Prosecution History: Response to Office Action, May 14, 2001, p. 2; Response to Office Action, May 14, 2001, p. 3; Response to Office Action, May 14, 2001, p. 6; Office Action, Jul. 26, 2001, p. 3; Response to Office Action, Oct. 26, 2001, p. 2; Final Office Action, Mar. 20, 2002, p. 3; Final Office Action, Mar. 20, 2002, p. 7; Final Office Action, Mar. 20, 2002, p. 8; RCE and Amendment, Aug. 15, 2002, p. 10; RCE	PROPOSED CONSTRUCTION: differing formats DICTIONARY/TREATISE DEFINITIONS: variant The American Heritage Dictionary of the English Language (4th Ed. 2000) adj. 1. Having or exhibiting variation; differing. 2. Tending or liable to vary; variable. 3. Deviating from a standard, usually by only a slight difference. EXPERT TESTIMONY: Realtek's expert, Dr. Nick Bambos, may provide testimony as to the definition of the disputed terms as would be understood by one of ordinary skill in the relevant art and may provide an explanation of the technology.

*Claim language (disputed terms in **bold**)*	*3Com's proposed construction and supporting evidence*	*Realtek's proposed construction and supporting evidence*
	and Amendment, Aug. 15, 2002, p. 11; RCE and Amendment, Aug. 15, 2002, p. 12; Office Action, Nov. 4, 2002, p. 5; Response to Office Action, Jan. 22, 2003, p. 11; Response to Office Action, Jan. 22, 2003, p. 12; Response to Office Action, Jan. 22, 2003, p. 13; Response to Office Action, Jan. 22, 2003, p. 14; Response to Office Action, Jan. 22, 2003, p. 15; Notice of Allowance, Feb. 2, 2003, p. 2. EXTRINSIC EVIDENCE: 3Com's expert, Dr. Michael Mitzenmacher may provide an expert report or other form of testimony regarding the technology to which this term relates and how a person having ordinary skill in the art in the field of networking technology would understand this term. 3Com reserves the right to rely on testimony by any expert in this action. See also U.S. Patent Nos. 5,434,872; 5,732,094; 6,327,625; 6,526,446; and 6,570,884; Joint Claim Construction Statement in Cv-05-00098 (VRW). 3Com reserves the right to rely on any statement made by any party under the Patent Local Rules.	

B. Claim Elements in Dispute as to Which Structures, Acts, or Materials the Elements Correspond Where the Parties Also Dispute Whether 35 U.S.C. § 112 ¶ 6 Applies

Claim element	*3Com's proposed structures, acts, or materials to which the elements correspond*	*D-Link's proposed structures, acts, or materials to which the elements correspond*	*Realtek's proposed structures, acts, or materials to which the elements correspond*
"means for comparing the counter to the threshold value in the alterable storage location and **generating an indication signal to the host processor responsive to a comparison of the counter and the alterable storage location**" found in claim numbers: '459 patent: 1	3Com contends that 35 U.S.C. § 112 ¶ 6 governs "**means for comparing**" (see Section C), but does not govern the additional limitation of "generating." To the extent the Court finds § 112 ¶ 6 applicable to "generating," each of the above disclosures of "means for comparing" are enabling with respect to the generation of an indication signal to a host processor, e.g., "**comparator 213**" outputs data to "**RCV COMPLETE control block 210**" (see fig. 14, col. 31, ln. 41), which generates an indication signal (see col 31, ln. 41-49); "**EARLY INDICATION LATCH block 512**" (see col. 38, ln. 51-55); "**early xmit complete block**" (see col. 39, ln 57); and "**AND gate 616**" (see fig. 31; col. 40, ln. 46); see also receive threshold logic (figs. 12a-18); transfer threshold logic (figs. 19-23); download transmit threshold logic (figs. 24-28); transmit threshold logic (figs. 29-34).	Fig. 14, comparator 213 and RCV complete control 210.	Realtek contends that 35 U.S.C. § 112 ¶ 6 governs both "means for comparing . . ." and "means for . . . generating an indication signal . . . ." and identifies the corresponding structures, acts, or materials as follows: Figs. 12a-18 – receive threshold logic Figs. 19-23 – transfer threshold logic Figs 24-28 – download transmit threshold logic Figs. 29-34 – transmit threshold logic
"**transmit logic, responsive to the means for initiating transmission, for retrieving data from the buffer memory**	This is not a "means-plus-function" claim element subject to construction under 35 U.S.C. § 112 ¶ 6. The use of the word "means" in claim drafting creates a presumption that § 112 ¶ 6 governs, while the absence of the word "means" in a	Transmit MAC logic 39 in Fig. 2; network interface processor 14 in Fig. 3; elements 50, 66, and 67 in Fig. 4 and 4A; Xmit DMA logic 109 in Fig. 5; transmit DMA logic 155 in Fig. 9; elements 320 and 321 in Fig. 12; elements 330, 331, and	Fig. 2 – transmit MAC Logic 39 Fig. 3 – network interface processor 14 Fig. 4 – RAM interface 50, transmit DMA 67, Ethernet transmitter 66

Claim element	*3Com's proposed structures, acts, or materials to which the elements correspond*	*D-Link's proposed structures, acts, or materials to which the elements correspond*	*Realtek's proposed structures, acts, or materials to which the elements correspond*
and supplying retrieved data for transmission on the communication medium" found in claim numbers: '872 patent: 1	particular claim element creates a presumption that § 112 ¶ 6 is inapplicable. The subject of this element, "transmit logic," is a well-known structure and its relationship to certain elements presumptively governed by § 112 ¶ 6 is not sufficient to bring it within the ambit of § 112 ¶ 6. To the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, such "transmit logic" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "**network adapter 6**" (see fig. 1; col. 4, ln. 2-4, 16-17); "**transmit logic 39**" (see fig. 2; col. 4, ln. 38); "**network adapter 6**" (see fig. 1; col. 4, ln. 2-4, 16-17); "**transmit DMA module 67**" (see figs. 4, 4A; col. 9, ln. 13-44); and "**Ethernet transmitter module 66**" (see fig.4; col. 9, ln. 45-51); see also network interface processor 14 (fig. 3); elements 50, 66, 67 (fig. 4 and 4A); Xmit DMA logic 109, transceiver 105 (fig. 5); transmit descriptors (fig. 7); transmit descriptor data structure (fig. 8); transmit descriptor ring buffer 152, transmit DMA logic 155 (fig. 9); elements 320 and 321 (fig. 12); elements 330, 331, and 332 (fig. 13); elements 335, 336, and 337 (fig. 14); elements 340, 341, and 342 (fig. 15); elements 350, 351, 353 [*sic*], 353, 354, 355, 356, and 357 (fig. 16), and elements 400,	332 in Fig. 13 elements 335, 336, and 337 in Fig. 14; elements 340, 341, and 342 in Fig. 15; elements 350, 351, 353 [*sic*], 353, 354, 355, 356, and 357 in Fig. 16, and elements 400, 405, 407, 410, 411, and 413 in Fig. 18.	Fig. 4A – transmit DMA 67 Fig. 5 – transmit DMA logic 109, transceiver 105 Fig. 7 – transmit descriptors Fig. 8 – transmit descriptor data structure Fig. 9 – transmit descriptor ring buffer 152, transmit DMA logic 155 Fig. 12 – data available control block 323 Fig. 17 – state machine elements 370, 371, 372, 373 Fig. 18 – transmit data path 400, paths 401, 402, MUX 410, transmit control logic 411

Claim element	*3Com's proposed structures, acts, or materials to which the elements correspond*	*D-Link's proposed structures, acts, or materials to which the elements correspond*	*Realtek's proposed structures, acts, or materials to which the elements correspond*
	405, 407, 410, 411, and 413 (fig. 18.) Fig. 12 – data available control block 323 Fig. 17 – state machine elements 370, 371, 372, 373 Fig. 18 – transmit data path 400, paths 401, 402, MUX 410, transmit control logic 411		
"**underrun control logic, which detects a condition in which the means for transferring falls behind the transmit logic, and supplies a bad frame signal to the communications medium in response to the underrun condition**" found in claim numbers: '872 patent: 1	This is not a "means-plus-function" claim element subject to construction under 35 U.S.C. § 112 ¶ 6. The use of the word "means" in claim drafting creates a presumption that § 112 ¶ 6 governs, while the absence of the word "means" in a particular claim element creates a presumption that § 112 ¶ 6 is inapplicable. The subject of this element, "underrun control logic," is a well-known structure and its relationship to certain elements presumptively governed by § 112 ¶ 6 is not sufficient to bring it within the ambit of § 112 ¶ 6. To the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, such "underrun control logic" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "**logic**" (see col. 2, ln. 30); "**host interface logic**" (see fig. 2; col. 4, ln. 57); an "**underrun detector**" (see fig. 18, col. 28, ln. 54); and "**XMIT FAILURE register**" (see col. 19, ln.14-38); see also	Underrun detector 413, and elements 405, 407, 410, and 411 in Fig. 18. "Communications Medium" A network path through which frames are transmitted or received.	Fig. 18 – CRC 404, exclusive OR gate 407, MUX 410, transmit control logic 411, underrun detector 413

Claim element	*3Com's proposed structures, acts, or materials to which the elements correspond*	*D-Link's proposed structures, acts, or materials to which the elements correspond*	*Realtek's proposed structures, acts, or materials to which the elements correspond*
	Underrun detector 413, and elements 404, 405, 407, 410, 411, 413 (fig. 18).		
"means, **coupled with the buffer memory and including a host system alterable threshold store for storing a threshold value,** for monitoring the transferring of data **of a frame to the buffer memory to make a threshold determination of an amount of data of the frame transferred to the buffer memory**" found in claim numbers: '872 patent: 10	While 3Com contends that 35 U.S.C. § 112 ¶ 6 governs "means . . . for monitoring [the transferring of data]" (see Section C), the limitation of "making a determination" is not governed by 35 U.S.C. § 112 ¶ 6. To the extent that the Court determines that this limitation is governed by 35 U.S.C. § 112 ¶ 6, the limitation is disclosed in the specification, without limitation, as: "**threshold logic 36**" (see fig. 2; col. 4, ln. 30-31, 40-41, 67); see also Early transmit logic 6A (fig. 1); threshold store 43 (fig. 2); network interface processor 14, RAM 15 (fig. 3); download DMA 58 (figs. 4 and 4A); transmit descriptor and download DMA logic 107 (fig. 5); elements 300, 301, 302, 303, 304, 305, 306, 307, 308, 309, 310, 311, 320, 321, 322, 323 (figs. 11 and 12); elements 330, 331, and 332 in Fig. 13; elements 335, 336, and 337 (fig. 14); elements 340, 341, and 342 (fig. 15); elements 350, 351, 352, 353, 354, 355, 356, 357 (fig. 16); and elements 370, 371, 372, and 373 (fig. 17). In addition, while the particular limitation of this element that requires that these means be coupled to the buffer memory and include a host system alterable threshold store are	Early transmit logic 6A in Fig. 1; threshold logic 36 in Fig. 2; network interface processor 14 in Fig. 3; download DMA 58 in Figs. 4 and 4A; elements 300, 301, 302, 303, 304, 305, 306, 307, 308, 309, 310, 311, 320, 321, 322, 323 in Figs. 11 and 12; elements 330, 331, and 332 in Fig. 13; elements 335, 336, and 337 in Fig. 14; elements 340, 341, and 342 of Fig. 15; elements 350, 351, 352, 353, 354, 355, 356, 357 in Fig. 16; and elements 370, 371, 372, and 373 in Fig. 17.	Fig. 2 – threshold logic 36, threshold store 43 Fig. 3 – RAM 15 Fig. 5 – transmit descriptor and download DMA logic 107 Fig. 11 – counter 300, AND Gate 301, delay circuit 302, adder 304, and D-type flip-flops 305, 206 Fig. 12 – start threshold register 320, download compare clock 321, and immediate data comparator 322 Fig. 13 – threshold registers 330, 331, and threshold valid register 332 Fig. 14 – threshold value state diagram elements 335-37 Fig. 15 – comparator 340, AND gate 341, comparator 342 Fig. 16 – counter 350, comparators 351-353, MUX 354, and gate 355, comparator 357

Claim element	*3Com's proposed structures, acts, or materials to which the elements correspond*	*D-Link's proposed structures, acts, or materials to which the elements correspond*	*Realtek's proposed structures, acts, or materials to which the elements correspond*
	not governed by 35 U.S.C. § 112 ¶ 6, such limitations are disclosed in connection with such means as "**threshold logic 36**" (see fig. 2; col. 4, ln. 30-31, 40-41), coupled to a threshold store which "in a preferred system, is dynamically programmable by the host computer 30." (see fig. 2; col. 4, ln. 46-47).		
"**data transfer circuitry, having a host system interface, for transferring data of frames to the buffer memory**" found in claim numbers: '872 patent: 21	This is not a "means-plus-function" claim element subject to construction under 35 U.S.C. § 112 ¶ 6. The use of the word "means" in claim drafting creates a presumption that § 112 ¶ 6 governs, while the absence of the word "means" in a particular claim element creates a presumption that § 112 ¶ 6 is inapplicable. To the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, such "data transfer circuitry" is disclosed in the specification and thereby enabled under 35 U.S.C. § 112 ¶ 6 by: "**line 35**" (see fig. 2; col. 4, ln. 30); see also Host interface logic 31, bus 2 (fig. 2); network interface processor 14, bus 13 (fig. 3); elements 50, 51, 53, 55, and 58, download DMA offset bus [12:2], download DMA byte enable [3.0] (figs. 4 and 4A); host interface logic 102, and Xmit descriptor and download DMA logic 107 (fig. 5); and host descriptor logic 150 and download DMA logic 151, transmit descriptor ring buffer 152 (fig. 9); adder 308, MUX	Host interface logic 31 in Fig. 2; network interface processor 14 in Fig. 3 (and specifically elements 50, 51, 53, 55, and 58 in Figs. 4 and 4A); host interface logic 102, and Xmit descriptor and download DMA logic 107 in Fig. 5; and host descriptor logic 150 and download DMA logic 151 in Fig. 9.	Fig. 2 – host interface 31, bus 2 Fig. 3 – network interface processor 14, bus 13 Fig. 4 – RAM interface 50, host bus interface 51, EISA bus master interface 55, master slave union 53, upload DMA 57, download DMA module 58 Fig. 4A – download DMA module 58, download DMA offset bus [12:2], download DMA byte enable [3.0] Fig. 5 – host interface logic 102, transmit descriptor logic, download DMA logic 107 Fig. 9 – host descriptor logic 150, download DMA logic 151, transmit descriptor ring buffer 152 Fig. 11 – adder 308, MUX 309, subtractor 310, register 311

Claim element	*3Com's proposed structures, acts, or materials to which the elements correspond*	*D-Link's proposed structures, acts, or materials to which the elements correspond*	*Realtek's proposed structures, acts, or materials to which the elements correspond*
	309, subtractor 310, register 311 (fig. 11).		
"**logic, coupled to the buffer memory, which monitors the transferring of data of a frame to the buffer memory to make a threshold determination of an amount of data of the frame transferred to the buffer memory**" found in claim numbers: '872 patent: 21	This is not a "means-plus-function" claim element subject to construction under 35 U.S.C. § 112 ¶ 6. The use of the word "means" in claim drafting creates a presumption that § 112 ¶ 6 governs, while the absence of the word "means" in a particular claim element creates a presumption that § 112 ¶ 6 is inapplicable. To the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, such "logic" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "**early transmit logic 6A**" (see fig. 1; col. 4, ln. 11); "**download DMA logic 58**" (see figs. 4, 4A; col. 23, ln. 22); "**11 bit counter 300**" (see fig. 11; col. 23, ln. 30); and "**download bytesResidentValue**" (see fig. 11; col. 24, ln. 9); see also threshold logic 36 (fig. 2); network interface processor 14 (fig. 3); elements 301, 302, 303, 304, 305, 306, 307, 308, 309, 310, 311, 320, 321, 323 (figs. 11 and 12); elements 330, 331, and 332 (fig. 13); elements 335, 336, and 337 (fig. 14); elements 340, 341, and 342 (fig. 15); elements 350, 351, 352, 353, 354, 355, 356, 357 (fig. 16); and elements 370, 371, 372, and 373 (fig. 17).	Early transmit logic 6A in Fig. 1, threshold logic 36 in Fig. 2; network interface processor 14 in Fig. 3; download DMA 58 in Figs. 4 and 4A; elements 300, 301, 302, 303, 304, 305, 306, 307, 308, 309, 310, 311, 320, 321, 323 in Figs. 11 and 12; elements 330, 331, and 332 of Fig. 13; elements 335, 336, and 337 of Fig. 14; elements 340, 341, and 342 of Fig. 15; elements 350, 351, 352, 353, 354, 355, 356, 357 in Fig. 16; and elements 370, 371, 372, and 373 in Fig. 17.	Figs. 11-12 – elements 300, 302, 303, 304, 305, 306, 307, 308, 309 310, 311, 320, 321, 322, and 323 Fig. 16 – elements 350, 351, 352, 353, 354, 355, 356, and 357
"**logic, responsive to**	This is not a "means-plus-function" claim element	Transmit MAC logic 39 in Fig. 2; network interface	Fig. 2 – threshold logic 36, threshold store 43

Claim element	*3Com's proposed structures, acts, or materials to which the elements correspond*	*D-Link's proposed structures, acts, or materials to which the elements correspond*	*Realtek's proposed structures, acts, or materials to which the elements correspond*
the threshold determination of the logic which monitors the transferring of data to the buffer memory, which initiates transmission of the frame from the buffer memory to the medium access controller prior to transfer of all of the data of the frame to the buffer memory, including logic which initiates transmission of the frame when no complete frame of data is present in the buffer memory" found in claim numbers: '872 patent: 21	subject to construction under 35 U.S.C. § 112 ¶ 6. The use of the word "means" in claim drafting creates a presumption that § 112 ¶ 6 governs, while the absence of the word "means" in a particular claim element creates a presumption that § 112 ¶ 6 is inapplicable. To the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, such "logic" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "**transmit logic 39**" (see fig. 2; col. 4, ln. 37-38); "**start threshold register 320**" (see fig. 12; col. 24, ln. 60-61); "**download compare block 321**" (see fig. 12; col. 24, ln. 61-62); "**immediate data comparator 322**" (see fig. 12; col. 24, ln. 64-65); and "**data available control block 323**" (see fig. 12; col. 24, ln. 67-68); see also threshold logic 36, threshold store 43 (fig. 2); network interface processor 14, RAM 15 (fig. 3); download DMA 58 (figs. 4 and 4A); transmit descriptor and download DMA logic 107 (fig. 5); counter 300, AND Gate 301, delay circuit 302, adder 304 and D-type flip-flops 305, 306 (fig. 11); elements 330, 331, and 332 (fig. 13); elements 335, 336, and 337 (fig. 14); elements 340, 341, and 342 (fig. 15); counter 350, comparators 351-353, MUX 354, and gate 355 comparator 357 (fig. 16);	processor 14 in Fig. 3; download DMA 58 in Figs. 4 and 4A; elements 320, 321, 322, and 323 in Fig. 12; elements 330, 331, and 332 in Fig. 13; elements 335, 336, and 337 of Fig. 14; elements 340, 341, and 342 of Fig. 15; elements 370, 371, 372, and 373 of Fig. 17, and elements 400, 405, 407, 410, 411, and 413 in Fig. 18. "Medium Access Controller" Circuitry or a device that controls access to the network.	Fig. 3 – RAM 15 Fig. 5 – transmit descriptor and download DMA logic 107 Fig. 11 – counter 300, AND Gate 301, delay circuit 302, adder 304 and D-type flip-flops 305, 306 Fig. 12 – start threshold register 320, download compare block 321, immediate data comparator 322 Fig. 13 – threshold registers 330, 331, and threshold valid register 332 Fig. 14 – threshold valid state diagram elements 335-337 Fig. 15 – comparator 340, AND gate 341, comparator 342 Fig. 16 – counter 350, comparators 351-353, MUX 354, and gate 355 comparator 357

Claim element	*3Com's proposed structures, acts, or materials to which the elements correspond*	*D-Link's proposed structures, acts, or materials to which the elements correspond*	*Realtek's proposed structures, acts, or materials to which the elements correspond*
	elements 370, 371, 372, and 373 (fig. 17); and elements 400, 405, 407, 410, 411, and 413 (fig. 18).		
"**logic to transfer packets out of the buffer to the other of the first and second ports according to the order of receipt, and according to the respective packet types so that packets having a particular packet type are transferred out of the order of receipt, relative to packets having another packet type**" found in claim numbers: '625 patent: 23	This is not a "means-plus-function" claim element subject to construction under 35 U.S.C. § 112 ¶ 6. The use of the word "means" in claim drafting creates a presumption that § 112 ¶ 6 governs, while the absence of the word "means" in a particular claim element creates a presumption that § 112 ¶ 6 is inapplicable. To the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, such "logic" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "**packet filter 14**" (see fig. 1; col. 4, ln. 13); "**FIFO(s) 13**" (see fig. 1; col. 4, ln. 2-5, 14); "**frame start header 16**" (see fig. 1; col. 4, ln. 15); "**frame start header 17**" (see fig. 1; col. 4, ln. 18); "**top packet data 18**" (see fig. 1; col. 4, ln. 18); "**IPsec queue 20**" (see fig. 1; col. 4, ln. 21); "**priority queue 21**" (see fig. 1; col. 4, ln. 21-22); "**packet download/receive control block 22**" (see fig. 1; col. 4, ln. 22-23); "**IPsec packet processing resources 23**" (see fig. 1; col. 4, ln. 25); "**packet upload/transmit control logic 24**" (see fig. 1; col. 4, ln. 26); "**out of order packet transfer control**		Fig. 1 – packet upload/transmit control 24, out of order packet transfer control 25, priority queue 21 Fig. 5 – elements 200, 201, 202, 203, 204, 205, and 206 Fig. 6 – elements 150, 151, 152, 153, 154, 155, 156, 157, 158, 159, 160, 161, 165, 167, 168, 169, 170, 171, 172, and 173 Fig. 8 – ASIC 814, filters and processing resources 830, upload engine 825

Claim element	*3Com's proposed structures, acts, or materials to which the elements correspond*	*D-Link's proposed structures, acts, or materials to which the elements correspond*	*Realtek's proposed structures, acts, or materials to which the elements correspond*
	block 25" (see fig. 1; col. 4, ln. 28); "**logic 26**" (see fig. 1; col. 4, ln. 29); "**logic 27**" (see fig. 1; col. 4, ln. 30); "**memory arbitration logic 28**" (see fig. 1; col. 4, ln. 34-35); "**multiplexer 29**" (see fig. 1; col. 4, ln. 35); "**idle state 100**" (see fig. 3; col. 5, ln. 10); "**state 101**" (see fig. 3; col. 5, ln. 12); "**state 102**" (see fig. 3; col. 5, ln. 14); "**branch 103**" (see fig. 3; col. 5, ln. 20); "**branch 104**" (see fig. 3; col. 5, ln. 21); "**branch 105**" (see fig. 3; col. 5, ln. 22); "**state 106**" (see fig. 3; col. 5, ln. 24); "**state 107**" (see fig. 3; col. 5, ln. 29); "**state 108**" (see fig. 3; col. 5, ln. 32); "**state 120**" (see fig. 4; col. 6, ln. 32); "**state 121**" (see fig. 4; col. 6, ln. 38); "**state 122**" (see fig. 4; col. 6, ln. 46); "**state 123**" (see fig. 4; col. 6, ln. 49); "**state 124**" (see fig. 4; col. 6, ln. 54); "**packet transmit/upload logic 24**" (see fig. 5; col. 7, ln 16); "**idle state 200**" (see fig. 5; col. 7, ln 17-18); "**state 201**" (see fig. 5; col. 7, ln 19); "**path 202**" (see fig. 5; col. 7, ln 25); "**align pointer state 203**" (see fig. 5; col. 7, ln 25); "**branch 204**" (see fig. 5; col. 7, ln 25); "**state 205**" (see fig. 5; col. 7, ln 26); "**data transfer state 206**" (see fig. 5; col. 7, ln 29); "**branch 207**" (see fig. 5; col. 7, ln 50); "**retransmit state 208**" (see fig. 5; col. 7, ln 51); "**branch 209**" (see fig. 5; col. 7, ln 55); "**flush state**		

Claim element	*3Com's proposed structures, acts, or materials to which the elements correspond*	*D-Link's proposed structures, acts, or materials to which the elements correspond*	*Realtek's proposed structures, acts, or materials to which the elements correspond*
	210" (see fig. 5; col. 7, ln 57); "**branch 211**" (see fig. 5; col. 7, ln 62); "**transfer complete state 212**" (see fig. 5; col. 7, ln 62-63); and "**resources 830**" (see fig. 8; col. 13, ln. 48); see also elements 150, 151, 152, 153, 154, 155, 156, 157, 158, 159, 160, 161, 165, 167, 168, 169, 170, 171, 172, and 173 (fig. 6); ASIC 814, filters and processing resources 830, upload engine 825 (fig. 8).		
"**second logic coupled with the buffer, and responsive to the packet filter to read and process data in the identified packets from the buffer, and to produce a data value dependent on contents of the packet prior to transfer of the identified packets to the second port by the first logic**" found in claim numbers: '884 patent: 1	This is not a "means-plus-function" claim element subject to construction under 35 U.S.C. § 112 ¶ 6. The use of the word "means" in claim drafting creates a presumption that § 112 ¶ 6 governs, while the absence of the word "means" in a particular claim element creates a presumption that § 112 ¶ 6 is inapplicable. To the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, such "second logic" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "**hardware filtering logic 15**" (see fig. 1; col. 4, ln. 16); "**embedded processor 14**" (see fig. 1; col. 4, ln. 15-16); "**line 18**" (see fig. 1; col. 4, ln. 26); "**embedded processor 118**" (see fig. 2; col. 5, ln. 8); "**pattern match modules, modules 203, 204, 205 and 206**" (see fig. 3; col. 5, ln. 43);		Fig. 1 – processor (slower) 14 Fig. 2 – processor (slower than data path) 118, including ARM 7 processor Fig. 3 – processor 220

Claim element	*3Com's proposed structures, acts, or materials to which the elements correspond*	*D-Link's proposed structures, acts, or materials to which the elements correspond*	*Realtek's proposed structures, acts, or materials to which the elements correspond*
	"**packet classify unit 210**" (see fig. 3; col. 5, ln. 44); "**receive FIFO control logic 218**" (see fig. 3; col. 6, ln. 29); "**processor 220**" (see fig. 3; col. 6, ln. 36); "**block 300**" (see fig. 4; col. 6, ln. 45); "**block 301**" (see fig. 4; col. 6, ln. 47-48); "**block 302**" (see fig. 4; col. 6, ln. 49); "**block 303**" (see fig. 4; col. 6, ln. 50); "**block 304**" (see fig. 4; col. 6, ln. 52); "**block 305**" (see fig. 4; col. 6, ln. 54); "**block 306**" (see fig. 4; col. 6, ln. 55); "**block 400**" (see fig. 5; col. 6, ln. 61); "**block 41**" (see col. 6, ln. 63); "**block 401**" (see fig. 5); "**block 402**" (see fig. 5; col. 6, ln. 64); "**block 403**" (see fig. 5; col. 7, ln. 2); "**block 404**" (see fig. 5; col. 7, ln. 5); "**block 405**" (see fig. 5; col. 7, ln. 7); "**block 406**" (see fig. 5; col. 7, ln. 8); "**ARM7 processor**" (col. 9, ln. 23); and "**general purpose processor module**" (see col. 11, ln. 29).		

C. Claim Elements that the Parties Agree Are Governed by 35 U.S.C. § 112 ¶ 6 but in Dispute as to Which Structures, Acts, or Materials the Elements Correspond

Claim element	*3Com's proposed structures, acts, or materials to which the elements correspond*	*D-Link's proposed structures, acts, or materials to which the elements correspond*	*Realtek's proposed structures, acts, or materials to which the elements correspond*
"**means for comparing the counter to the threshold value in the**	"Means for comparing" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "**logic**		Fig. 2, includes without limitation – threshold logic 10, alterable storage location 10a, host processor 5, network adaptor 3

Claim element	*3Com's proposed structures, acts, or materials to which the elements correspond*	*D-Link's proposed structures, acts, or materials to which the elements correspond*	*Realtek's proposed structures, acts, or materials to which the elements correspond*
alterable storage location" found in claim numbers: '459 patent: 1	**block 219**" (see fig. 14; col. 32, ln. 3); "**comparator 213**" (see fig. 14; col. 32, ln. 25-26); "**comparator 224**" (see fig. 14; col. 32, ln. 46); "**comparator 318**" (see fig. 21; col. 36, ln. 15); "**comparator 333**" (fig. 23; col. 37, ln. 40); "**THRESHOLD COMPARE block 511**" (see fig. 24, 26; col. 38, ln. 42, 44); "**comparator 517**" (see fig. 26; col. 38, ln. 2-5); "**comparator 615**" (see fig. 31; col. 40, ln. 41-45); see also threshold logic 10, alterable storage location 10a, host processor 5, network adaptor 3 (fig. 2); register 221, counter 216, logic block 218, register 223, comparator 224, logic block 222 (figs. 12a-18); comparator 318 (figs. 19-23); adder 614 (figs. 29-34).		Figs. 12a-18, includes without limitation – register 221, counter 216, logic block 218, comparator 213, register 223, comparator 224, logic block 222 Figs. 19-23, includes without limitation. adder 317, comparator 318 Figs. 24-28, includes without limitation comparator 333 Figs. 29-34, includes without limitation, adder 614, comparator 615
"**means … for transferring [data]**" found in claim numbers: '872 patent: 1	The "means" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "**host interface logic 31**" (see fig. 2; col. 4, ln. 29; col. 5, ln. 20); "**download DMA module 58**" (see fig. 4; col. 8, ln. 55-col. 9, ln. 11); and "**XMIT AREA register**" (see col. 18, ln. 6-10); see also network interface processor 14 (fig. 3); elements 50, 51, 53, 54, and 55 (figs. 4 and 4A); host interface logic 102 and Xmit descriptor and download DMA logic 107 (fig. 5); and host descriptor logic 150 and download DMA logic 151 (fig. 9).	Host interface logic 31 in Fig. 2; network interface processor 14 in Fig. 3; elements 50, 51, 53, 54, 55, and 58 in Figs. 4 and 4A; host interface logic 102 and Xmit descriptor and download DMA logic 107 in Fig. 5; and host descriptor logic 150 and download DMA logic 151 in Fig. 9.	See "means, having a host system interface, for transferring data of frames to the buffer memory."

Claim element	*3Com's proposed structures, acts, or materials to which the elements correspond*	*D-Link's proposed structures, acts, or materials to which the elements correspond*	*Realtek's proposed structures, acts, or materials to which the elements correspond*
"**means, having a host system interface, for transferring data of frames to the buffer memory**" found in claim numbers: '872 patent: 1	The "means" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "**host interface logic 31**" (see fig. 2; col. 4, ln. 29; col. 5, ln. 20); "**download DMA module 58**" (see fig. 4; col. 8, ln. 55-col. 9, ln. 11); and "**XMIT AREA register**" (see col. 18, ln. 6-10); see also bus 2 (fig. 1); host interface 31, bus 2 (fig. 2); network interface processor 14, bus 13 (fig. 3); elements 50, 51, 53, 54, and 55, and download DMA offset bus [12:2], download DMA byte enable [3:0] (figs. 4 and 4A); host interface logic 102 and Xmit descriptor and download DMA logic 107 (fig. 5); and host descriptor logic 150, download DMA logic 151, and transmit descriptor ring buffer 152 (fig. 9).	Host interface logic 31 in Fig. 2; network interface processor 14 in Fig. 3; elements 50, 51, 53, 54, 55, and 58 in Figs. 4 and 4A; host interface logic 102 and Xmit descriptor and download DMA logic 107 in Fig. 5; and host descriptor logic 150 and download DMA logic 151 in Fig. 9.	Fig. 1 – bus 2 Fig. 2 – host interface 31, bus 2 Fig. 3 – network interface processor 14, bus 13 Fig. 4 – RAM interface 50, host bus interface 51, EISA bus master interface 55, master slave union 53, download DMA module 57 Fig. 4A – download DMA module 58, download DMA offset bus [12:2], download DMA byte enable [3:0] Fig. 5 – host interface logic 102, transmit descriptor and download DMA logic 107 Fig. 9 – host descriptor logic 150, download DMA logic 151, transmit descriptor ring buffer 152
"**means … for monitoring [the transferring of data]**" found in claim numbers: '872 patent: 1	The "means" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "**threshold logic 36**" (see fig. 2; col. 4, ln. 30-31, 40-41); "**early transmit logic 6A**" (see fig. 1; col. 4, ln. 11); "**download DMA logic 58**" (see figs. 4, 4A; col. 23, ln. 22); "**11 bit counter 300**" (see fig. 11; col. 23, ln. 30); and "**download bytesResidentValue**" (see fig. 11; col. 24, ln. 9); see also network interface processor 14 (fig. 3); elements 301, 302, 303, 304, 305, 306, 307, 308, 309, 310, 311, 320, 321, 322, 323 (figs. 11 and 12); elements	Early transmit logic 6A in Fig. 1; threshold logic 36 in Fig. 2; network interface processor 14 in Fig. 3; download DMA 58 in Figs. 4 and 4A; elements 300, 301, 302, 303, 304, 305, 306, 307, 308, 309, 310, 311, 320, 321, 322, 323 in Figs. 11 and 12; elements 330, 331, and 332 in Fig. 13; elements 335, 336, and 337 in Fig. 14; elements 340, 341, and 342 of Fig. 15; elements 350, 351, 352, 353, 354, 355, 356, 357 in Fig. 16; and elements 370, 371, 372, and 373 in Fig. 17. "Monitoring"	See "means, coupled with the buffer memory and including a host system alterable threshold store for storing a threshold value, for monitoring the transferring of data of a frame to the buffer memory to make a threshold determination of an amount of data of the frame transferred to the buffer memory."

Claim element	*3Com's proposed structures, acts, or materials to which the elements correspond*	*D-Link's proposed structures, acts, or materials to which the elements correspond*	*Realtek's proposed structures, acts, or materials to which the elements correspond*
	330, 331, and 332 (fig. 13); elements 335, 336, and 337 (fig. 14); elements 340, 341, and 342 (fig. 15); elements 350, 351, 352, 353, 354, 355, 356, 357 (fig. 16); and elements 370, 371, 372, and 373 (fig. 17).	Watching, keeping track of, or checking on. Reference: 7, 12	
"**means … for initiating [transmission]**" found in claim numbers: '872 patent: 1	The "means" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "**transmit logic 39**" (see fig. 2; col. 4, ln. 37-38); "**start threshold register 320**" (see fig. 12; col. 24, ln. 60-61); "**download compare block 321**" (see fig. 12; col. 24, ln. 61-62); "**immediate data comparator 322**" (see fig. 12; col. 24, ln. 64-65); and "**data available control block 323**" (see fig. 12; col. 24, ln. 67-68); see also network interface processor 14 (fig. 3); download DMA 58 (figs. 4 and 4A); elements 330, 331, and 332 of Fig. 13; elements 335, 336, and 337 of Fig. 14; elements 340, 341, and 342 (fig 15); elements 370, 371, 372, and 373 (fig. 17); and elements 400, 405, 407, 410, 411, and 413 (fig. 18).	Transmit MAC logic 39 of Fig. 2; network interface processor 14 in Fig. 3; download DMA 58 in Figs. 4 and 4A; elements 320, 321, 322, and 323 in Fig. 12; elements 330, 331, and 332 of Fig. 13; elements 335, 336, and 337 of Fig. 14; elements 340, 341, and 342 of Fig 15; elements 370, 371, 372, and 373 of Fig. 17; and elements 400, 405, 407, 410, 411, and 413 in Fig. 18.	See "means, responsive to the threshold determination of the means for monitoring, for initiating transmission of the frame, prior to transfer of all the data of the frame to the buffer memory from the host computer."
"**means, responsive to the threshold determination of the means for monitoring, for initiating transmission of the frame prior to transfer of all the data**	The "means" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "**transmit logic 39**" (see fig. 2; col. 4, ln. 37-38); "**start threshold register 320**" (see fig. 12; col. 24, ln. 60-61); "**download compare block 321**" (see fig. 12; col. 24, ln. 61-62); "**immediate data comparator 322**" (see fig.	Transmit MAC logic 39 of Fig. 2; network interface processor 14 in Fig. 3; download DMA 58 in Figs. 4 and 4A; elements 320, 321, 322, and 323 in Fig. 12; elements 330, 331, and 332 of Fig. 13; elements 335, 336, and 337 of Fig. 14; elements 340, 341, and 342 of Fig 15; elements 370, 371, 372, and 373 of Fig. 17;	Fig. 1 – early transmit logic 6A Fig. 2 – transmit MAC logic Fig. 3 – network interface processor Fig. 4 & 4A – transmit DMA 67 Fig. 5 – network interface

Claim element	*3Com's proposed structures, acts, or materials to which the elements correspond*	*D-Link's proposed structures, acts, or materials to which the elements correspond*	*Realtek's proposed structures, acts, or materials to which the elements correspond*
of the frame to the buffer memory from the host computer" found in claim numbers: '872 patent: 1	12; col. 24, ln. 64-65); and "**data available control block 323**" (see fig. 12; col. 24, ln. 67-68); see also early transmit logic 6A (fig. 1); transmit MAC logic (fig. 2); network interface processor 14 (fig. 3); download DMA 58 and transmit DMA 67 (figs. 4 and 4A); network interface logic 104 (fig. 5); transmit descriptor ring buffer 152, transmit DMA logic 155 (fig. 9); elements 330, 331, and 332 (fig. 13); elements 335, 336, and 337 (fig. 14); elements 340, 341, and 342 (fig. 15); elements 370, 371, 372, and 373 (fig. 17); and elements 400, 405, 407, 410, 411, and 413 (fig. 18).	and elements 400, 405, 407, 410, 411, and 413 in Fig. 18. "Monitoring" Watching, keeping track of, or checking on. Reference: 7, 12	logic 104 Fig. 9 – transmit descriptor ring buffer 152, transmit DMA logic 155 Fig. 12 – data available control block 323 Fig. 17 – state machine elements 370, 371, 372, 373 Fig. 18 – transmit data path 400, data paths 401-402, MUX 410 and transmit control logic 411.
"**[host interface] means … for transferring [data]**" found in claim numbers: '872 patent: 10	The "means" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "**host interface logic 31**" (see fig. 2; col. 4, ln. 29; col. 5, ln. 20); "**download DMA module 58**" (see fig. 4; col. 8, ln. 55-col. 9, ln. 11); and "**XMIT AREA register**" (see col. 18, ln. 6-10); see also network interface processor 14 (fig. 3); elements 50, 51, 53, 54, and 55 (figs. 4 and 4A); host interface logic 102 (including Xmit descriptor and download DMA logic 107 and View, Xfer, and Upload DMA logic 108) (fig. 5); host descriptor logic 150 and download DMA logic 151 (fig. 9).	Host interface logic 31 in Fig. 2; network interface processor 14 in Fig. 3 (and specifically elements 50, 51, 53, 54, 55, and 58 in Figs. 4 and 4A); host interface logic 102 (including Xmit descriptor and download DMA logic 107 and View, Xfer, and Upload DMA logic 108) in Fig. 5; and host descriptor logic 150 and download DMA logic 151 in Fig. 9.	See "host interface means, having an interface to the host system, for transferring data between the host system and the buffer memory."
"**host interface means, having an interface to**	The "means" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes,	Host interface logic 31 in Fig. 2; network interface processor 14 in Fig. 3 (and	Fig. 2 – host interface 31, bus 2

Claim element	*3Com's proposed structures, acts, or materials to which the elements correspond*	*D-Link's proposed structures, acts, or materials to which the elements correspond*	*Realtek's proposed structures, acts, or materials to which the elements correspond*
the host system, for transferring data between the host system and the buffer memory" found in claim numbers: '872 patent: 10	without limitation: "**host interface logic 31**" (see fig. 2; col. 4, ln. 29; col. 5, ln. 20); "**download DMA module 58**" (see fig. 4; col. 8, ln. 55-col. 9, ln. 11); and "**XMIT AREA register**" (see col. 18, ln. 6-10); see also host interface 31, bus 2 (fig. 2); network interface processor 14, bus 13 (fig. 3); elements 50, 51, 53, 55, and 57, download DMA offset bus [12:2], download DMA byte enable [3.0] (figs. 4 and 4A); host interface logic 102 (including Xmit descriptor and download DMA logic 107 and View, Xfer, and Upload DMA logic 108) (fig. 5); transmit area (fig. 6); transmit descriptors (fig. 7); host descriptor logic 150, download DMA logic 151, transmit descriptor ring buffer 152 (fig. 9); adder 308, MUX 309, subtractor 310, and register 311 (fig. 11).	specifically elements 50, 51, 53, 55, 57, and 58 in Figs. 4 and 4A); host interface logic 102 (including Xmit descriptor and download DMA logic 107 and View, Xfer, and Upload DMA logic 108) in Fig. 5; host descriptor logic 150 and download DMA logic 151 in Fig. 9.	Fig. 3 – network interface processor 14, bus 13 Fig. 4 – RAM interface 50, host bus interface 51, EISA bus master interface 55, master slave union 53, upload DMA 57, download DMA module 58 Fig. 4A – download DMA module 58, download DMA offset bus [12:2], download DMA byte enable [3.0] Fig. 5 – host interface logic 102, transmit descriptor logic and download DMA logic 107 Fig. 6 – transmit area Fig. 7 – transmit descriptors Fig. 9 – host descriptor logic 150, download DMA logic 151, transmit descriptor ring buffer 152 Fig. 11 – adder 308, MUX 309, subtractor 310, and register 311
"**means, coupled with the buffer memory and including a host system alterable threshold store for storing a threshold value, for monitoring the transferring of data of a frame to the buffer memory to make a threshold**	The "means for monitoring" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "**threshold logic 36**" (see fig. 2; col. 4, ln. 30-31, 40-41); "**early transmit logic 6A**" (see fig. 1; col. 4, ln. 11); "**download DMA logic 58**" (see figs. 4, 4A; col. 23, ln. 22); "**11 bit counter 300**" (see fig. 11; col. 23, ln. 30); and "**download bytesResidentValue**" (see fig. 11; col. 24, ln. 9); see also threshold store 43 (fig.	Early transmit logic 6A in Fig. 1; threshold logic 36 in Fig. 2; network interface processor 14 in Fig. 3; download DMA 58 in Figs. 4 and 4A; elements 300, 301, 302, 303, 304, 305, 306, 307, 308, 309, 310, 311, 320, 321, 322, 323 in Figs. 11 and 12; elements 330, 331, and 332 in Fig. 13; elements 335, 336, and 337 in Fig. 14; elements 340, 341, and 342 of Fig. 15; elements 350, 351, 352, 353, 354, 355, 356, 357 in Fig.	Fig. 2 – threshold logic 36, threshold store 43 Fig. 3 – RAM 15 Fig. 5 – transmit descriptor and download DMA logic 107 Fig. 11 – counter 300, AND Gate 301, delay circuit 302, adder 304, and D-type flip-flops 305, 206 Fig. 12 – start threshold register 320, download

Claim element	*3Com's proposed structures, acts, or materials to which the elements correspond*	*D-Link's proposed structures, acts, or materials to which the elements correspond*	*Realtek's proposed structures, acts, or materials to which the elements correspond*
determination of an amount of data of the frame transferred to the buffer memory" found in claim numbers: '872 patent: 10	2); network interface processor 14, RAM 15 (fig. 3); transmit descriptor and download DMA logic 107 (fig. 5); elements 300, 301, 302, 303, 304, 305, 306, 307, 308, 309, 310, 311, 320, 321, 322, 323 (figs. 11 and 12); elements 330, 331, and 332 (fig. 13); elements 335, 336, and 337 (fig. 14); elements 340, 341, and 342 (fig. 15); elements 350, 351, 352, 353, 354, 355, 356, 357 (fig. 16); elements 370, 371, 372, and 373 (fig. 17). Other limitations in this element are not governed by 35 U.S.C. § 112 ¶ 6. See subsection II.A.2 supra.	16; and elements 370, 371, 372, and 373 in Fig. 17.	compare clock 321, and immediate data comparator 322 Fig. 13 – threshold registers 330, 331, and threshold valid register 332 Fig. 14 – threshold value state diagram elements 335-37 Fig. 15 – comparator 340, AND gate 341, comparator 342 Fig. 16 – counter 350, comparators 351-353, MUX 354, and gate 355, comparator 357
"**means, responsive to the threshold determination of the means for monitoring, for initiating transmission of the frame, prior to transfer of all the data of the frame to the buffer memory from the host computer**" found in claim numbers: 1 '872 patent:	The "means" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "**transmit logic 39**" (see fig. 2; col. 4, ln. 37-38); "**start threshold register 320**" (see fig. 12; col. 24, ln. 60-61); "**download compare block 321**" (see fig. 12; col. 24, ln. 61-62); "**immediate data comparator 322**" (see fig. 12; col. 24, ln. 64-65); and "**data available control block 323**" (see fig. 12; col. 24, ln. 67-68); see also early transmit logic 6A (fig. 1); network interface processor 14 in (fig. 3); download DMA 58 (figs. 4 and 4A); transmit descriptor ring buffer 152, transmit DMA logic 155 (fig. 9); data available control block 323 (fig. 12); elements 330, 331, and 332 (fig. 13); elements 335, 336, and 337 (fig. 14);	Transmit MAC logic 39 of Fig. 2; network interface processor 14 in Fig. 3; download DMA 58 in Figs. 4 and 4A; elements 320, 321, 322, and 323 in Fig. 12; elements 330, 331, and 332 of Fig. 13; elements 335, 336, and 337 of Fig. 14; elements 340, 341, and 342 of Fig 15; elements 370, 371, 372, and 373 of Fig. 17; and elements 400, 405, 407, 410, 411, and 413 in Fig. 18. "Monitoring" Watching, keeping track of, or checking on. Reference: 7, 12	Fig. 1 – early transmit logic 6A Fig. 9 – transmit descriptor ring buffer 152, transmit DMA logic 155 Fig. 12 – data available control block 323 Fig. 17 – state machine elements 370, 371, 372, 373 Fig. 18 – transmit data path 400, data paths 401-402, MUX 410 and transmit control logic 411.

Claim element	*3Com's proposed structures, acts, or materials to which the elements correspond*	*D-Link's proposed structures, acts, or materials to which the elements correspond*	*Realtek's proposed structures, acts, or materials to which the elements correspond*
	elements 340, 341, and 342 (fig 15); elements 370, 371, 372, and 373 (fig. 17); elements 400, 401, 402, 405, 407, 410, 411, and 413 (fig. 18).		
"**[network interface] means … for transferring [data]**" found in claim numbers: '872 patent: 10	The "network interface means" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "**transmit logic 39**" (see fig. 2; col. 4, ln. 38); "**transmit DMA module 67**" (see figs. 4, 4A; col. 9, ln. 13-44); "**Ethernet transmitter module 66**" (see fig.4; col. 9, ln. 45-51); "**Ethernet receiver module 62**" (see fig.4; col. 9, ln. 53-59); "**receive DMA module 63**" (see figs. 4, 4A; col. 9, ln. 60-col. 10, ln. 12); and "**upload DMA module 57**" (see figs. 4, 4A; col. 10, ln. 13-37); see also network interface processor 14 (fig. 3); elements 50 and 66 (figs. 4 and 4A); Xmit DMA logic 155 (fig. 9); elements 320 and 321 (fig. 12); elements 330, 331, and 332 (fig. 13); elements 335, 336, and 337 (fig. 14); elements 340, 341, and 342 (fig. 15); elements 350, 351, 352, 353, 354, 355, 356, and 357 (fig. 16); and elements 400, 405, 407, 410, 411, and 413 (fig. 18).	Transmit MAC logic 39 of Fig. 2; network interface processor 14 in Fig. 3; elements 50, 66, and 67 in Fig. 4 and 4A; Xmit DMA logic 155 in Fig. 9, elements 320 and 321 in Fig. 12; elements 330, 331, and 332 in Fig. 13; elements 335, 336, and 337 in Fig. 14; elements 340, 341, and 342 in Fig. 15; elements 350, 351, 353 [*sic*], 353, 354, 355, 356, and 357 in Fig. 16, and elements 400, 405, 407, 410, 411, and 413 in Fig. 18. "Network" A system of computers, terminals, and databases connected by communications paths. Reference: 7, 12	See "network interface means, having an interface to the network transceiver and responsive to the means for initiating, for transferring data between the buffer memory and the network transceiver for transmission."
"**network interface means, having an interface to the network transceiver and responsive to the means for initiating,**	The "network interface means" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "**network adapter 6**" (see fig. 1; col. 4, ln. 2-4, 16-17); "**transmit DMA module 67**" (see figs. 4, 4A; col. 9,	Transmit MAC logic 39 of Fig. 2; network interface processor 14 in Fig. 3; download DMA 58 in Figs. 4 and 4A; elements 320, 321, 322, and 323 in Fig. 12; elements 330, 331, and 332 of Fig. 13; elements 335, 336, and 337 of Fig. 14;	Fig. 3 – network interface processor 14, encoder/decoder 19 Fig. 4 – cycle arbiter 56, interrupt controller 60, Ethernet transmitter 66, and transmit DMA 67 Fig. 4A – transmit DMA 67 Fig. 5 – transmit DMA

Claim element	*3Com's proposed structures, acts, or materials to which the elements correspond*	*D-Link's proposed structures, acts, or materials to which the elements correspond*	*Realtek's proposed structures, acts, or materials to which the elements correspond*
for transferring data between the buffer memory and the network transceiver for transmission" found in claim numbers: '872 patent: 10	ln. 13-44); "**Ethernet transmitter module 66**" (see fig.4; col. 9, ln. 45-51); "**Ethernet receiver module 62**" (see fig.4; col. 9, ln. 53-59); "**receive DMA module 63**" (see figs. 4, 4A; col. 9, ln. 60-col. 10, ln. 12); and "**upload DMA module 57**" (see figs. 4, 4A; col. 10, ln. 13-37); see also Transmit MAC logic 39 (fig. 2); network interface processor 14 and encoder/decoder 19 (fig. 3); cycle arbiter 56, download DMA 58, interrupt controller 60, Ethernet transmitter 66, and transmit DMA 67 (figs. 4 and 4A); transmit DMA Logic 109 (fig. 5); transmit descriptors (fig. 7); transmit descriptor ring buffer 152, transmit DMA logic 155 (fig. 9); elements 320, 321, 322, and 323 (fig. 12); elements 330, 331, and 332 (fig. 13); elements 335, 336, and 337 (fig. 14); elements 340, 341, and 342 (fig. 15); elements 370, 371, 372, and 373 (fig. 17); elements 400, 401, 402 405, 407, 410, 411, and 413 (fig. 18).	elements 340, 341, and 342 of Fig. 15; elements 370, 371, 372, and 373 of Fig. 17; and elements 400, 405, 407, 410, 411, and 413 in Fig. 18. "Network" A system of computers, terminals, and databases connected by communications paths. Reference: 7, 12	Logic 109 Fig. 7 – transmit descriptors Fig. 9 – transmit descriptor ring buffer 152, transmit DMA logic 155 Fig. 18 – transmit data path 400, data paths 401-402, MUX 410 and transmit control logic 411
"**[control] means … for posting [status information]**" found in claim numbers: '872 patent: 10	The "means for posting" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "**logic**" (see col. 2, ln. 30); "**host interface logic**" (see fig. 2; col. 4, ln. 57); an "**underrun detector**" (see fig. 18, col. 28, ln. 54); and "**XMIT FAILURE register**" (see col. 19, ln.14-38); see also Info and Status registers (fig. 6).	Info and Status registers in Fig. 6; underrun detector 413 in Fig. 18.	See "control means, coupled with the network interface means, for posting status information for use by the host system, as feedback for optimizing the threshold value."

Claim element	*3Com's proposed structures, acts, or materials to which the elements correspond*	*D-Link's proposed structures, acts, or materials to which the elements correspond*	*Realtek's proposed structures, acts, or materials to which the elements correspond*
"**control means, coupled with the network interface means, for posting status information for use by the host system, as feedback for optimizing the threshold value**" found in claim numbers: '872 patent: 10	The "means for posting" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "**logic**" (see col. 2, ln. 30); "**host interface logic**" (see fig. 2; col. 4, ln. 57); an "**underrun detector**" (see fig. 18, col. 28, ln. 54); and "**XMIT FAILURE register**" (see col. 19, ln.14-38); see also Info and Status registers (fig. 6); and transmit control logic 411 (fig. 18).	Info and Status registers in Fig. 6; underrun detector 413 in Fig. 18.	Fig. 18 – transmit control logic 411 and underrun detector 413.

D. Claim Elements as to Which the Parties are in Dispute as to Whether 35 U.S.C. § 112 ¶ 6 Governs, but in Hypothetical Agreement as to Which Structures, Acts, or Materials the Elements Would Correspond

Claim element	*Structures, acts, or materials to which the elements correspond*	*3Com's position as to whether §112 ¶ 6 governs*	*D-Link's position as to whether §112 ¶ 6 governs*	*Realtek's position as to whether §112 ¶ 6 governs*
"**first logic coupled with the buffer and the second port, to transfer packets from the buffer to the second port**" found in claim numbers:	To the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, such "first logic" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "**upload engine 116**" (see fig. 2) and "**load engine**	This is not a "means-plus-function" claim element subject to construction under 35 U.S.C. § 112 ¶ 6. The use of the word "means" in claim drafting creates a presumption that § 112 ¶ 6 governs, while the absence of the word "means" in a particular claim	*§112 ¶ 6 governs*	*§112 ¶ 6 governs*

'884 patent: 1	**116**" (see col. 4, ln. 64-65).	element creates a presumption that § 112 ¶ 6 is inapplicable.		

In accordance with the Court's Standing Order 3.0, the parties attach copies of the 5, 307,459, 5,434,872, 5,732,094, 6,327,625, 6,526,446, and 6,570,884 patents as Exhibits D through I, respectively. The parties also make a complete prosecution history for each of these patents available to the Court upon request.

III. PATENT L.R. 4-3(c): TIME FOR CLAIM CONSTRUCTION HEARING

The parties believe that one day will be sufficient for the Claim Construction Hearing.

IV. PATENT L.R. 4-3(d): WITNESSES AT CLAIM CONSTRUCTION HEARING

Pursuant to Patent L.R. 4-3(d) and Standing Order 3.2, the parties understand that the court will not receive live testimony in connection with this claim construction hearing. Attached are summaries of opinions to be offered by 3Com Corporation's expert, by Realtek Semiconductor Corp.'s experts Drs. Izhak Rubin and Nick Bambos, and a statement from D-Link Systems Inc.'s expert Mr. Howard Frazier, at Exhibits A-C respectively.

V. PATENT L.R. 4-3(e): OTHER ISSUES FOR PRE-CLAIM CONSTRUCTION HEARING CONFERENCE

The parties have not identified any other issues which might appropriately be taken up at a prehearing conference prior to the Claim Construction Hearing.

Dated: January 18, 2006

Respectfully Submitted,

SIMPSON THACHER & BARTLETT LLP
By: \s\Henry B. Gutman
Henry B. Gutman (admitted *pro hac vice*)

Attorneys for Plaintiff/Counterdefendant
3Com Corporation

Dated: January 18, 2006

Respectfully Submitted,

AKIN GUMP STRAUSS HAUER & FELD LLP
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Attorneys for Defendant/Counterplaintiff
Realtek Semiconductor Corp.

Dated: January 18, 2006

Respectfully Submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.
By: \s\ Steven H. Morrissett
Steven H. Morrissett (CSB No. 073424)

Attorneys for Defendant/Counterplaintiff
D-Link Systems, Inc.

Pursuant to General Order No. 45, Section X(B) regarding signatures, I attest under penalty of perjury that concurrence in the filing of this document has been obtained from Elizabeth H. Rader and Steven H. Morrissett.

Dated: January 18, 2006

SIMPSON THACHER & BARTLETT LLP
By: \s\ Henry B. Gutman
Henry B. Gutman (admitted *pro hac vice*)

Attorneys for Plaintiff/Counterdefendant

EXHIBIT A

STATEMENT OF 3COM CORP.'S EXPERT, DR. MICHAEL MITZENMACHER

A. QUALIFICATIONS

Dr. Michael Mitzenmacher graduated *summa cum laude* with a degree in mathematics and computer science from Harvard in 1991. After studying math for a year in Cambridge, England, on the Churchill Scholarship, Dr. Mitzenmacher obtained his Ph.D. in computer science at University of California at Berkley in 1996. Dr. Mitzenmacher then worked at Digital Systems Research Center until joining the Harvard faculty in 1999.

Dr. Mitzenmacher is a Professor of Computer Science in the Division of Engineering and Applied Sciences at Harvard University. Dr. Mitzenmacher has authored or co-authored over 100 conference and journal publications on a variety of topics, including Internet algorithms, hashing, load-balancing, erasure codes, error-correcting codes, compression, bin-packing, and power laws. Dr. Mitzenmacher's work on low-density parity-check codes shared the 2002 IEEE Information Theory Society Best Paper Award. Dr. Mitzenmacher's first textbook on probabilistic techniques in computer science, co-written with Eli Upfal, was published in 2005 by Cambridge University Press.

B. TESTIMONY

1. Level of Ordinary Skill in the Art

3Com may provide an expert report from Dr. Mitzenmacher regarding the general purpose and use of network interface cards and Ethernet networking technology, as well as the specific network interface cards of the patents-in-suit. Dr. Mitzenmacher's report may also provide information as to the level of experience, knowledge, and skill typical of a person having ordinary skill in those arts concerned with the technology disclosed in the patents-in-suit and how the terms proposed collectively by both sides in this action for construction are used by a person

having ordinary skill in the art, and specifically how such a person would interpret such terms in the context of the respective specifications, claims and prosecution histories of the patents-in-suit.

Such an expert report may further provide information as to the structure(s), act(s), and/or material(s), and equivalents thereof, disclosed in the respective specifications of the patents-in-suit or known to a person having ordinary skill in the art for each claim element found by the court to be governed by 35 U.S.C. § 112(6).

2. The Meaning of Claims Terms

The following section details Dr. Mitzenmacher's opinions regarding how one of ordinary skill in the art in the field of networking technology would understand the disputed claim terms:

a. "**alterable storage location**"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this term, as it appears in U.S. Patent No. 5,307,459, should be construed to mean "storage location whose value is changeable."

b. "**buffer**"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this term, as it appears in U.S. Patent Nos. 5,307,459, 5,434,872, 5,732,094, 6,327,625, and 6,570,884, should be construed to mean "A memory for temporary storage of data."

c. "**buffer memory**"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the

art, Dr. Mitzenmacher will assert that this phrase, as it appears in U.S. Patent Nos. 5,307,459, 5,434,872, and 5,732,094, should be construed to mean "A memory for temporary storage of data."

d. "**indication signal**"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this phrase, as it appears in U.S. Patent No. 5,307,459, should be construed to mean "a signal that indicates a subsequent action, such as an interrupt."

e. "**logic**"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this term, as it appears in U.S. Patent Nos. 5,307,459, 5,434,872, 6,327,625, and 6,570,884, should be construed to mean "circuitry and/or programming."

f. "**threshold value**"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this phrase, as it appears in U.S. Patent Nos. 5,307,459, 5,434,872, and 5,732,094, should be construed to mean "a value representing the quantity of data sufficient to trigger the initiation of transmission."

g. "**falls behind**"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this phrase, as it appears in U.S. Patent No. 5,434,872,

should be construed to mean "underruns."

h. "**a condition in which the means for transferring falls behind the transmit logic**"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this phrase, as it appears in U.S. Patent No. 5,434,872, should be construed to mean "a transmission underrun condition."

i. "**underrun**"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this term, as it appears in U.S. Patent Nos. 5,434,872 and 5,732,094, should be construed to mean "When expected data from a frame to be transferred is not available."

j. "**underrun control logic**"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this phrase, as it appears in U.S. Patent No. 5,434,872, should be construed to mean "logic that detects underruns."

k. "**bad frame signal**"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this phrase, as it appears in U.S. Patent Nos. 5,434,872 and 5,732,094, should be construed to mean "a signal that a frame is bad."

l. "**feedback**"

In light of his review of the patent, prosecution history, and specification, in

connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this term, as it appears in U.S. Patent Nos. 5,434,872 and 5,732,094, should be construed to mean "information from output returned to the input."

m. "**optimizing the threshold**"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this phrase, as it appears in U.S. Patent Nos. 5,434,872 and 5,732,094, should be construed to mean "attempting to make the transmission of frames more efficient."

n. "**logic which initiates transmission of the frame when no complete frame of data is present in the buffer memory**"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this phrase, as it appears in U.S. Patent No. 5,434,872, should be construed to mean "threshold logic that begins transmission of a frame before all data in the frame is within the buffer memory."

o. "**threshold amount of data**"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this phrase, as it appears in U.S. Patent No. 5,732,094, should be construed to mean "an amount representing the quantity of data of a frame sufficient to trigger the initiation of transmission."

p. "**altering the threshold**"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the

art, Dr. Mitzenmacher will assert that the underlined term, as it appears in U.S. Patent No. 5,732,094, should be construed to mean "changing."

q. "**logic to transfer packets out of the buffer**"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this phrase, as it appears in U.S. Patent No. 6,327,625, should be construed to mean "circuitry and/or programming to transfer packets out of the buffer."

r. "**order of receipt**"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this phrase, as it appears in U.S. Patent No. 6,327,625, should be construed to mean "order of receipt."

s. "**packet types**"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this phrase, as it appears in U.S. Patent No. 6,327,625, should be construed to mean "packets with different formats and priorities."

t. "**transfer packets out of the buffer to the other of the first and second ports according to the order of receipt, and according to the respective packet types**"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this phrase, as it appears in U.S. Patent No. 6,327,625, should be construed to mean "data frames are transferred to the other of the host and the network

from the buffer within each packet type according to the order of receipt."

u. "**data download circuit**"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this phrase, as it appears in U.S. Patent No. 6,526,446, should be construed to mean "a circuit that retrieves data."

v. "**descriptor signal**"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this phrase, as it appears in U.S. Patent No. 6,526,446, should be construed to mean "a signal that describes data."

w. "**a descriptor signal which corresponds to data stored within memory**"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this phrase, as it appears in U.S. Patent No. 6,526,446, should be construed to mean "the descriptor signal describes the data stored within host memory."

x. "**frame segment descriptor**"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this phrase, as it appears in U.S. Patent No. 6,526,446, should be construed to mean "a descriptor for a frame segment."

y. "**data value**"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the

art, Dr. Mitzenmacher will assert that this phrase, as it appears in U.S. Patent No. 6,570,884, should be construed to mean "a value of bit(s) of data."

z. "**first logic**"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this phrase, as it appears in U.S. Patent No. 6,570,884, should be construed to mean "first circuits and/or programming."

aa. "**read and process data in the identified packets from the buffer**"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this phrase, as it appears in U.S. Patent No. 6,570,884, should be construed to mean "read and process data in the identified packets from the buffer."

bb. "**second logic**"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this phrase, as it appears in U.S. Patent No. 6,570,884, should be construed to mean "second circuits and/or programming."

cc. "**variant formats**"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, Dr. Mitzenmacher will assert that this phrase, as it appears in U.S. Patent No. 6,570,884, should be construed to mean "varying arrangements of packet information other than a destination MAC address."

dd. "**means for comparing the counter to the threshold value in the alterable storage location and <u>generating an indication signal to</u>**

the host processor responsive to a comparison of the counter and the alterable storage location"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Mitzenmacher will assert that, as it appears in U.S. Patent No. 5,307,459, such "means" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "comparator 213" outputs data to "**RCV COMPLETE control block 210**" (see fig. 14, col. 31, ln. 41), which generates an indication signal (see col 31, ln. 41-49); "**EARLY INDICATION LATCH block 512**" (see col. 38, ln. 51-55); "**early xmit complete block**" (see col. 39, ln 57); and "**AND gate 616**" (see fig. 31; col. 40, ln. 46).

ee. "**transmit logic, responsive to the means for initiating transmission, for retrieving data from the buffer memory and supplying retrieved data for transmission on the communication medium**"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Mitzenmacher will assert that, as it appears in U.S. Patent No. 5,434,872, such "transmit logic" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "**network adapter 6**" (see fig. 1; col. 4, ln. 2-4, 16-17); "**transmit logic 39**" (see fig. 2; col. 4, ln. 38); "**network adapter 6**" (see fig. 1; col. 4, ln. 2-4, 16-17); "**transmit DMA module 67**" (see figs. 4, 4A; col. 9, ln. 13-44); and "**Ethernet transmitter module 66**" (see fig.4; col. 9, ln. 45-51).

ff. "**underrun control logic, which detects a condition in which the means for transferring falls behind the transmit logic, and supplies a bad frame signal to the communications medium in response to the underrun condition**"

In light of his review of the patent, prosecution history, and specification, in

connection with his knowledge of how such terms are used by a person having ordinary skill in the art, to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Mitzenmacher will assert that, as it appears in U.S. Patent No. 5,434,872, such "underrun control logic" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "**logic**" (see col. 2, ln. 30); "**host interface logic**" (see fig. 2; col. 4, ln. 57); an "**underrun detector**" (see fig. 18, col. 28, ln. 54); and "**XMIT FAILURE register**" (see col. 19, ln.14-38).

gg. "**means, coupled with the buffer memory and including a host system alterable threshold store for storing a threshold value, for monitoring the transferring of data of a frame to the buffer memory to make a threshold determination of an amount of data of the frame transferred to the buffer memory**"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Mitzenmacher will assert that, as it appears in U.S. Patent No. 5,434,872, such "means" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "**threshold logic 36**" (see fig. 2; col. 4, ln. 30-31, 40-41, 67).

In addition, while the particular limitation of this element that requires that these means be coupled to the buffer memory and include a host system alterable threshold store are not governed by 35 U.S.C. § 112 ¶ 6, such limitations are disclosed in connection with such means as "**threshold logic 36**" (see fig. 2; col. 4, ln. 30-31, 40-41), coupled to a threshold store which "in a preferred system, is dynamically programmable by the host computer 30." (see fig. 2; col. 4, ln. 46-47).

hh. "**data transfer circuitry, having a host system interface, for transferring data of frames to the buffer memory**"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the

art, to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Mitzenmacher will assert that, as it appears in U.S. Patent No. 5,434,872, such "data transfer circuitry" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "**line 35**" (see fig. 2; col. 4, ln. 30).

ii. "**logic, coupled to the buffer memory, which monitors the transferring of data of a frame to the buffer memory to make a threshold determination of an amount of data of the frame transferred to the buffer memory**"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Mitzenmacher will assert that, as it appears in U.S. Patent No. 5,434,872, such "logic" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "**early transmit logic 6A**" (see fig. 1; col. 4, ln. 11); "**download DMA logic 58**" (see figs. 4, 4A; col. 23, ln. 22); "**11 bit counter 300**" (see fig. 11; col. 23, ln. 30); and "**download bytesResidentValue**" (see fig. 11; col. 24, ln. 9).

jj. "**logic, responsive to the threshold determination of the logic which monitors the transferring of data to the buffer memory, which initiates transmission of the frame from the buffer memory to the medium access controller prior to transfer of all of the data of the frame to the buffer memory, including logic which initiates transmission of the frame when no complete frame of data is present in the buffer memory**"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Mitzenmacher will assert that, as it appears in U.S. Patent No. 5,434,872, such "logic" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "**transmit logic 39**" (see fig. 2; col. 4, ln. 37-38); "**start threshold register 320**" (see fig. 12; col. 24, ln. 60-61);

"**download compare block 321**" (see fig. 12; col. 24, ln. 61-62); "**immediate data comparator 322**" (see fig. 12; col. 24, ln. 64-65); and "**data available control block 323**" (see fig. 12; col. 24, ln. 67-68).

kk. "**logic to transfer packets out of the buffer to the other of the first and second ports according to the order of receipt, and according to the respective packet types so that packets having a particular packet type are transferred out of the order of receipt, relative to packets having another packet type**"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Mitzenmacher will assert that, as it appears in U.S. Patent No. 6,327,625, such "logic" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "**packet filter 14**" (see fig. 1; col. 4, ln. 13); "**FIFO(s) 13**" (see fig. 1; col. 4, ln. 2-5, 14); "**frame start header 16**" (see fig. 1; col. 4, ln. 15); "**frame start header 17**" (see fig. 1; col. 4, ln. 18); "**top packet data 18**" (see fig. 1; col. 4, ln. 18); "**IPsec queue 20**" (see fig. 1; col. 4, ln. 21); "**priority queue 21**" (see fig. 1; col. 4, ln. 21-22); "**packet download/receive control block 22**" (see fig. 1; col. 4, ln. 22-23); "**IPsec packet processing resources 23**" (see fig. 1; col. 4, ln. 25); "**packet upload/transmit control logic 24**" (see fig. 1; col. 4, ln. 26); "**out of order packet transfer control block 25**" (see fig. 1; col. 4, ln. 28); "**logic 26**" (see fig. 1; col. 4, ln. 29); "**logic 27**" (see fig. 1; col. 4, ln. 30); "**memory arbitration logic 28**" (see fig. 1; col. 4, ln. 34-35); "**multiplexer 29**" (see fig. 1; col. 4, ln. 35); "**idle state 100**" (see fig. 3; col. 5, ln. 10); "**state 101**" (see fig. 3; col. 5, ln. 12); "**state 102**" (see fig. 3; col. 5, ln. 14); "**branch 103**" (see fig. 3; col. 5, ln. 20); "**branch 104**" (see fig. 3; col. 5, ln. 21); "**branch 105**" (see fig. 3; col. 5, ln. 22); "**state 106**" (see fig. 3; col. 5, ln. 24); "**state 107**" (see fig. 3; col. 5, ln. 29); "**state 108**" (see fig. 3; col. 5, ln. 32); "**state 120**" (see fig. 4; col. 6, ln. 32); "**state 121**" (see fig. 4; col. 6, ln. 38); "**state 122**" (see fig. 4; col. 6, ln. 46);

"**state 123**" (see fig. 4; col. 6, ln. 49); "**state 124**" (see fig. 4; col. 6, ln. 54); "**packet transmit/upload logic 24**" (see fig. 5; col. 7, ln 16); "**idle state 200**" (see fig. 5; col. 7, ln 17-18); "**state 201**" (see fig. 5; col. 7, ln 19); "**path 202**" (see fig. 5; col. 7, ln 25); "**align pointer state 203**" (see fig. 5; col. 7, ln 25); "**branch 204**" (see fig. 5; col. 7, ln 25); "**state 205**" (see fig. 5; col. 7, ln 26); "**data transfer state 206**" (see fig. 5; col. 7, ln 29); "**branch 207**" (see fig. 5; col. 7, ln 50); "**retransmit state 208**" (see fig. 5; col. 7, ln 51); "**branch 209**" (see fig. 5; col. 7, ln 55); "**flush state 210**" (see fig. 5; col. 7, ln 57); "**branch 211**" (see fig. 5; col. 7, ln 62); "**transfer complete state 212**" (see fig. 5; col. 7, ln 62-63); and "**resources 830**" (see fig. 8; col. 13, ln. 48).

ll. "**second logic coupled with the buffer, and responsive to the packet filter to read and process data in the identified packets from the buffer, and to produce a data value dependent on contents of the packet prior to transfer of the identified packets to the second port by the first logic**"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Mitzenmacher will assert that, as it appears in U.S. Patent No. 6,570,884, such "second logic" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "**hardware filtering logic 15**" (see fig. 1; col. 4, ln. 16); "**embedded processor 14**" (see fig. 1; col. 4, ln. 15-16); "**line 18**" (see fig. 1; col. 4, ln. 26); "**embedded processor 118**" (see fig. 2; col. 5, ln. 8); "**pattern match modules, modules 203, 204, 205 and 206**" (see fig. 3; col. 5, ln. 43); "**packet classify unit 210**" (see fig. 3; col. 5, ln. 44); "**receive FIFO control logic 218**" (see fig. 3; col. 6, ln. 29); "**processor 220**" (see fig. 3; col. 6, ln. 36); "**block 300**" (see fig. 4; col. 6, ln. 45); "**block 301**" (see fig. 4; col. 6, ln. 47-48); "**block 302**" (see fig. 4; col. 6, ln. 49); "**block 303**" (see fig. 4; col. 6, ln. 50); "**block 304**" (see fig. 4; col. 6, ln. 52); "**block 305**" (see fig. 4; col. 6, ln. 54); "**block 306**" (see fig. 4; col. 6, ln. 55); "**block 400**" (see fig. 5; col. 6, ln. 61); "**block 41**" (see col.

6, ln. 63); "**block 401**" (see fig. 5); "**block 402**" (see fig. 5; col. 6, ln. 64); "**block 403**" (see fig. 5; col. 7, ln. 2); "**block 404**" (see fig. 5; col. 7, ln. 5); "**block 405**" (see fig. 5; col. 7, ln. 7); "**block 406**" (see fig. 5; col. 7, ln. 8); "**ARM7 processor**" (col. 9, ln. 23); and "**general purpose processor module**" (see col. 11, ln. 29).

mm. "**means for comparing the counter to the threshold value in the alterable storage location**"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Mitzenmacher will assert that, as it appears in U.S. Patent No. 5,307,459, such "means for comparing" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "**logic block 219**" (see fig. 14; col. 32, ln. 3); "**comparator 213**" (see fig. 14; col. 32, ln. 25-26); "**comparator 224**" (see fig. 14; col. 32, ln. 46); "**comparator 318**" (see fig. 21; col. 36, ln. 15); "**comparator 333**" (fig. 23; col. 37, ln. 40); "**THRESHOLD COMPARE block 511**" (see fig. 24, 26; col. 38, ln. 42, 44); "**comparator 517**" (see fig. 26; col. 38, ln. 2-5); "**comparator 615**" (see fig. 31; col. 40, ln. 41-45).

nn. "**means … for transferring [data]**"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Mitzenmacher will assert that, as it appears in U.S. Patent No. 5,434,872, such "means for transferring" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "**host interface logic 31**" (see fig. 2; col. 4, ln. 29; col. 5, ln. 20); "**download DMA module 58**" (see fig. 4; col. 8, ln. 55-col. 9, ln. 11); and "**XMIT AREA register**" (see col. 18, ln. 6-10).

oo. "**means, having a host system interface, for transferring data of frames to the buffer memory**"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Mitzenmacher will assert that, as it appears in U.S. Patent No. 5,434,872, such "means for transferring" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "**host interface logic 31**" (see fig. 2; col. 4, ln. 29; col. 5, ln. 20); "**download DMA module 58**" (see fig. 4; col. 8, ln. 55-col. 9, ln. 11); and "**XMIT AREA register**" (see col. 18, ln. 6-10).

pp. "**means … for monitoring [the transferring of data]**"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Mitzenmacher will assert that, as it appears in U.S. Patent No. 5,434,872, such "means for monitoring" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "**threshold logic 36**" (see fig. 2; col. 4, ln. 30-31, 40-41); "**early transmit logic 6A**" (see fig. 1; col. 4, ln. 11); "**download DMA logic 58**" (see figs. 4, 4A; col. 23, ln. 22); "**11 bit counter 300**" (see fig. 11; col. 23, ln. 30); and "**download bytesResidentValue**" (see fig. 11; col. 24, ln. 9).

qq. "**means … for initiating [transmission]**"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Mitzenmacher will assert that, as it appears in U.S. Patent No. 5,434,872, such "means for initiating" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "**transmit logic 39**" (see fig. 2; col. 4, ln. 37-38); "**start threshold register 320**" (see fig. 12; col.

24, ln. 60-61); "**download compare block 321**" (see fig. 12; col. 24, ln. 61-62); "**immediate data comparator 322**" (see fig. 12; col. 24, ln. 64-65); and "**data available control block 323**" (see fig. 12; col. 24, ln. 67-68).

rr. "**means, responsive to the threshold determination of the means for monitoring, for initiating transmission of the frame prior to transfer of all the data of the frame to the buffer memory from the host computer**"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Mitzenmacher will assert that, as it appears in U.S. Patent No. 5,434,872, such "means for monitoring" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "**transmit logic 39**" (see fig. 2; col. 4, ln. 37-38); "**start threshold register 320**" (see fig. 12; col. 24, ln. 60-61); "**download compare block 321**" (see fig. 12; col. 24, ln. 61-62); "**immediate data comparator 322**" (see fig. 12; col. 24, ln. 64-65); and "**data available control block 323**" (see fig. 12; col. 24, ln. 67-68).

ss. "**[host interface] means … for transferring [data]**"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Mitzenmacher will assert that, as it appears in U.S. Patent No. 5,434,872, such "means" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "**host interface logic 31**" (see fig. 2; col. 4, ln. 29; col. 5, ln. 20); "**download DMA module 58**" (see fig. 4; col. 8, ln. 55-col. 9, ln. 11); and "**XMIT AREA register**" (see col. 18, ln. 6-10).

tt. "**host interface means, having an interface to the host system, for transferring data between the host system and the buffer memory**"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Mitzenmacher will assert that, as it appears in U.S. Patent No. 5,434,872, such "data transfer circuitry" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "**host interface logic 31**" (see fig. 2; col. 4, ln. 29; col. 5, ln. 20); "**download DMA module 58**" (see fig. 4; col. 8, ln. 55-col. 9, ln. 11); and "**XMIT AREA register**" (see col. 18, ln. 6-10).

uu. "**means, coupled with the buffer memory and including a host system alterable threshold store for storing a threshold value, for monitoring the transferring of data of a frame to the buffer memory to make a threshold determination of an amount of data of the frame transferred to the buffer memory**"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Mitzenmacher will assert that, as it appears in U.S. Patent No. 5,434,872, such "means for monitoring" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "**threshold logic 36**" (see fig. 2; col. 4, ln. 30-31, 40-41); "**early transmit logic 6A**" (see fig. 1; col. 4, ln. 11); "**download DMA logic 58**" (see figs. 4, 4A; col. 23, ln. 22); "**11 bit counter 300**" (see fig. 11; col. 23, ln. 30); and "**download bytesResidentValue**" (see fig. 11; col. 24, ln. 9).

vv. "**means, responsive to the threshold determination of the means for monitoring, for initiating transmission of the frame, prior to transfer of all the data of the frame to the buffer memory from the host computer**"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr.

Mitzenmacher will assert that, as it appears in U.S. Patent No. 5,434,872, such "means for initiating" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "**transmit logic 39**" (see fig. 2; col. 4, ln. 37-38); "**start threshold register 320**" (see fig. 12; col. 24, ln. 60-61); "**download compare block 321**" (see fig. 12; col. 24, ln. 61-62); "**immediate data comparator 322**" (see fig. 12; col. 24, ln. 64-65); and "**data available control block 323**" (see fig. 12; col. 24, ln. 67-68).

ww. "**[network interface] means … for transferring [data]**"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Mitzenmacher will assert that, as it appears in U.S. Patent No. 5,434,872, such "network interface means" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "**transmit logic 39**" (see fig. 2; col. 4, ln. 38); "**transmit DMA module 67**" (see figs. 4, 4A; col. 9, ln. 13-44); "**Ethernet transmitter module 66**" (see fig.4; col. 9, ln. 45-51); "**Ethernet receiver module 62**" (see fig.4; col. 9, ln. 53-59); "**receive DMA module 63**" (see figs. 4, 4A; col. 9, ln. 60-col. 10, ln. 12); and "**upload DMA module 57**" (see figs. 4, 4A; col. 10, ln. 13-37).

xx. "**network interface means, having an interface to the network transceiver and responsive to the means for initiating, for transferring data between the buffer memory and the network transceiver for transmission**"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Mitzenmacher will assert that, as it appears in U.S. Patent No. 5,434,872, such "network interface means" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "**network adapter 6**" (see fig. 1; col. 4, ln. 2-4, 16-17); "**transmit DMA module 67**" (see figs. 4,

4A; col. 9, ln. 13-44); "**Ethernet transmitter module 66**" (see fig.4; col. 9, ln. 45-51); "**Ethernet receiver module 62**" (see fig.4; col. 9, ln. 53-59); "**receive DMA module 63**" (see figs. 4, 4A; col. 9, ln. 60-col. 10, ln. 12); and "**upload DMA module 57**" (see figs. 4, 4A; col. 10, ln. 13-37).

yy. "**[control] means … for posting [status information]**"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Mitzenmacher will assert that, as it appears in U.S. Patent No. 5,434,872, such "means for posting" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "**logic**" (see col. 2, ln. 30); "**host interface logic**" (see fig. 2; col. 4, ln. 57); an "**underrun detector**" (see fig. 18, col. 28, ln. 54); and "**XMIT FAILURE register**" (see col. 19, ln.14-38).

zz. "**control means, coupled with the network interface means, for posting status information for use by the host system, as feedback for optimizing the threshold value**"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Mitzenmacher will assert that, as it appears in U.S. Patent No. 5,434,872, such "means for posting" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "**logic**" (see col. 2, ln. 30); "**host interface logic**" (see fig. 2; col. 4, ln. 57); an "**underrun detector**" (see fig. 18, col. 28, ln. 54); and "**XMIT FAILURE register**" (see col. 19, ln.14-38).

aaa. "**first logic coupled with the buffer and the second port, to transfer packets from the buffer to the second port**"

In light of his review of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr.

Mitzenmacher will assert that, as it appears in U.S. Patent No. 6,570,884, such "first logic" disclosed in the specification under 35 U.S.C. § 112 ¶ 6 includes, without limitation: "**upload engine 116**" (see fig. 2) and "**load engine 116**" (see col. 4, ln. 64-65).

C. CONCLUSION

Dr. Mitzenmacher reserves the right to respond to any opinions put forth by Realtek Semiconductor Corp. or D-Link Systems Inc. in expert reports, during deposition, trial or otherwise, as well as any further documents, evidence or information regarding claims construction and to supplement this statement accordingly.

EXHIBIT B

I. SUMMARY OF TESTIMONY OF DR. IZHAK RUBIN IN SUPPORT OF REALTEK'S POSITIONS SET FORTH IN THE JOINT CLAIM CONSTRUCTION AND PREHEARING STATEMENT PURSUANT TO PATENT LOCAL RULE 4-3

A. QUALIFICATIONS

Dr. Izhak Rubin received his Bachelor of Science and Master of Science degrees from the Technion – Israel Institute of Technology, Haifa, Israel, in 1964 and 1968, respectively, and his Ph.D. degree from Princeton University, Princeton, NJ, in 1970, all in Electrical Engineering. During 1964-1967, he served as a Communications Engineer and Officer in the Israeli Signal Corps. In 1967-1968, he worked as an Electronics and C3 Engineer in the Israel Aircraft Industries. Since 1970, he has been on the faculty of the University of California, Los Angeles ("UCLA"), School of Engineering and Applied Science, where he is currently a Professor in the Electrical Engineering Department.

Dr. Rubin has had extensive research, publications, consulting, and industrial experience in the design and analysis of commercial and military computer communications and telecommunications systems and networks. At UCLA, he is leading a large research group. He also serves as President of IRI Computer Communications Corporation, a company engaged in software development and consulting services.

During 1979-1980, Dr. Rubin served as Acting Chief Scientist of the Xerox Telecommunications Network. He served as co-chairman of the 1981 IEEE International Symposium on Information Theory; as program chairman of the 1984 NSF-UCLA workshop on Personal Communications; as program chairman for the 1987 IEEE INFOCOM conference; and as program co-chair of the IEEE 1993 workshop on Local and Metropolitan Area networks. Dr. Rubin is a Fellow of Institute of Electrical and Electronics Engineers ("IEEE"), a prestigious and international professional organization, the most distinguished membership grade bestowed by the

IEEE and awarded only to a limited number of its distinguished members. He has been serving as an editor of the IEEE Transactions on Communications, of the ACM/Baltzer journal on Wireless Networks, of the Optical Networks magazine, of the Photonic Network Communications journal, and of the Communications Systems journal. He has contributed chapters to texts on telecommunications systems and networks.

B. GENERAL TESTIMONY

Dr. Rubin may be called to testify as Realtek's expert regarding the general purpose and use of network interface cards or controller chips and Ethernet networking technology, as well as the products involved the patents-in-suit. He may also testify as to the level of experience, knowledge, and skill typical of a person having ordinary skill in those arts concerned with the technology disclosed in the patents-in-suit and how the terms proposed collectively by both sides in this action for construction are used by a person having ordinary skill in the art, and specifically how such a person would interpret such terms in the context of the respective specifications, claims, and prosecution histories of the patents-in-suit. Dr. Rubin may also testify as to the structure(s), act(s), and/or material(s), and equivalents or lack thereof, disclosed in the respective specifications of the patents-in-suit or known to a person having ordinary skill in the art for each claim element found by the court to be governed by 35 U.S.C. § 112(6).

C. TESTIMONY ON CLAIM CONSTRUCTION

Dr. Rubin may provide written or oral testimony on the following matters:

1. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term, "alterable storage location," as it appears in claim 1 of U.S. Patent No. 5,307,459, to mean "storage location whose value is dynamically changeable."

2. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the terms "buffer" and "buffer memory," as each appears in claim 1 of U.S. Patent No. 5,307,459, claims 1, 10, and 21 of U.S. Patent No. 5,434,872, and claims 1, 9, 21, 28, 39, and 47 of U.S. Patent No. 5,732,094, to mean "a memory that (1) stores frame data such that the frame data can be retrieved independently of the order in which the frame data were stored and the frame data can always be retained and reused and can be accessed by the host system; and (2) is not a first-in-first-out (FIFO) system."

3. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term, "indication signal," as it appears in claim 1 of U.S. Patent No. 5,307,459, to mean "a signal that is not an interrupt, but may be used by the host system to generate an interrupt."

4. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term, "logic," as it appears in claims 1 and 21 of U.S. Patent No. 5,434,872; claim 1 of U.S. Patent No. 5,307,459; to mean "a device," should the Court determine that the term should not be construed under 35 U.S. C. § 112 ¶ 6.

5. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term, "threshold value," as it appears in claim 1 of U.S. Patent No. 5,307,459, claim 10 of U.S. Patent No. 5,434,872, and claim 47 of U.S. Patent No. 5,732, 094, to mean "a number corresponding to a level of data required for some process to take place."

6. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term, "falls behind," as it appears in claim 1 of U.S.

Patent No. 5,434,872, to mean "a condition in which the transferring of data by the host interface falls behind the transferring of data by a transmit logic."

7. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term, "a condition in which the means for transferring falls behind the transmit logic," as it appears in claim 1 of U.S. Patent No. 5,434,872, to mean "a condition in which the transferring of data into a transmit data buffer by the host interface falls behind the transferring of data into a transmit data path by a transmit logic."

8. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term, "underrun" and "falls behind" as each appears in claim 1 of U.S. No. 5,434,872 and claim 21 of U.S. Patent No. 5,732,094, to have the same meaning as "falls behind," which means "a condition in which the transferring of data into a transmit data buffer by the host interface falls behind the transferring of data into a transmit data path by a transmit logic."

9. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term, "underrun control logic," as it appears in claim 1 of U.S. Patent No. 5,434,872, to mean "device for controlling underrun," should the Court determine that the term should not be construed under 35 U.S. C. § 112 ¶ 6.

10. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term, "bad frame signal," as it appears in claim 1 of U.S. No. 5,434,872 and claim 21 of U.S. Patent No. 5,732,094, to mean "a signal indicating that a frame is bad."

11. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term, "feedback," as it appears in claim 10 of U.S. No. 5,434,872 and claims 21 and 47 of U.S. Patent No. 5,732,094, to mean "information from output that is returned to input."

12. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term, "optimizing the threshold," as it appears in claim 10 of U.S. No. 5,434,872 and claim 21 of U.S. Patent No. 5,732,094, to mean "dynamically changing the threshold value by the host system to make it as perfect, effective, or functional as possible."

13. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term, "threshold amount of data," as it appears in claim 21 of U.S. Patent No. 5,732,094, to mean "the amount of data required for some process to take place."

14. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term, "altering the threshold," as it appears in claim 47 of U.S. Patent No. 5,732,094, to mean "dynamically changing the threshold."

15. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term "logic", as it appears in many claimed elements of claims 1 and 21 of U.S. Patent No. 5,434,872 and claim 1 of U.S. Patent No. 5,307,459, as lacking suggestion or indication of specific structure.

16. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term "underrun control logic," as it appears in claim 1 of U.S. Patent No. 5,434,872, as lacking suggestion or indication of specific structure.

17. In light of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, and to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Rubin proposes to testify that the term, "means for comparing the counter to the threshold value in the alterable storage location and generating an indication signal to the host processor responsive to a comparison of the counter and the alterable storage location," as it appears in claim 1 of U.S. Patent No. 5,307,459 and as disclosed in the specification under 35 U.S.C. § 112 ¶ 6, includes, without limitation: Figs. 12a-18 — receive threshold logic; Figs. 19-23 — transfer threshold logic; Figs 24-28 — download transmit threshold logic; Figs 29-34 — transmit threshold logic.

18. In light of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, and to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Rubin proposes to testify that the term, "transmit logic, responsive to the means for initiating transmission, for retrieving data from the buffer memory and supplying retrieved data for transmission on the communication medium," as it appears in claim 1 of U.S. Patent No. 5,434,872 and as disclosed in the specification under 35 U.S.C. § 112 ¶ 6, includes, without limitation: Fig. 2 – transmit MAC Logic 39; Fig. 3 – network interface processor 14; Fig. 4 – RAM interface 50, transmit DMA 67, Ethernet transmitter 66; Fig. 4A – transmit DMA 67; Fig. 5 – transmit DMA logic 109, transceiver 105; Fig. 7 – transmit descriptors; Fig. 8 – transmit descriptor data structure; Fig. 9 – transmit descriptor ring buffer 152, transmit DMA logic 155; Fig. 12 – data available control block 323;

Fig. 17 – state machine elements 370, 371, 372, 373; Fig. 18 – transmit data path 400, paths 401, 402, MUX 410, transmit control logic 411.

19. In light of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, and to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Rubin proposes to testify that the term, "means for comparing the counter to the threshold value in the alterable storage location and generating an indication signal to the host processor responsive to a comparison of the counter and the alterable storage location," as it appears in claim 1 of U.S. Patent No. 5,434,872 and as disclosed in the specification under 35 U.S.C. § 112 ¶ 6, includes, without limitation: Figs. 12a-18 – receive threshold logic, Figs. 19-23 – transfer threshold logic, Figs 24-28 – download transmit threshold logic, Figs. 29-34 – transmit threshold logic.

20. In light of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, and to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Rubin proposes to testify that the term, "underrun control logic, which detects a condition in which the means for transferring falls behind the transmit logic, and supplies a bad frame signal to the communications medium in response to the underrun condition," as it appears in claim 1 of U.S. Patent No. 5,434,872 and as disclosed in the specification under 35 U.S.C. § 112 ¶ 6, includes, without limitation: Fig. 18 – CRC 404, exclusive OR gate 407, MUX 410, transmit control logic 411, underrun detector 413.

21. In light of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, and to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Rubin proposes

to testify that the term, "means, coupled with the buffer memory and including a host system alterable threshold store for storing a threshold value, for monitoring the transferring of data of a frame to the buffer memory to make a threshold determination of an amount of data of the frame transferred to the buffer memory," as it appears in claim 10 of U.S. Patent No. 5,434,872 and as disclosed in the specification under 35 U.S.C. § 112 ¶ 6, includes, without limitation: Fig. 2 – threshold logic 36, threshold store 43; Fig. 3 – RAM 15; Fig. 5 – transmit descriptor and download DMA logic 107; Fig. 11 – counter 300, AND Gate 301, delay circuit 302, adder 304, and D-type flip-flops 305, 206; Fig. 12 – start threshold register 320, download compare clock 321, and immediate data comparator 322; Fig. 13 – threshold registers 330, 331, and threshold valid register 332; Fig. 14 – threshold value state diagram elements 335-37; Fig. 15 – comparator 340, AND gate 341, comparator 342; Fig. 16 – counter 350, comparators 351-353, MUX 354, and gate 355, comparator 357.

22. In light of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, and to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Rubin proposes to testify that the term, "data transfer circuitry, having a host system interface, for transferring data of frames to the buffer memory," as it appears in claim 21 of U.S. Patent No. 5,434,872 and as disclosed in the specification under 35 U.S.C. § 112 ¶ 6, includes, without limitation: Fig. 2 – host interface 31, bus 2; Fig. 3 – network interface processor 14, bus 13; Fig. 4 – RAM interface 50, host bus interface 51, EISA bus master interface 55, master slave union 53, upload DMA 57, download DMA module 58; Fig. 4A – download DMA module 58, download DMA offset bus [12:2], download DMA byte enable [3.0]; Fig. 5 – host interface logic 102, transmit descriptor logic, download DMA logic 107; Fig. 9 – host descriptor logic 150, download DMA logic 151, transmit descriptor ring buffer 152; Fig. 11 – adder 308, MUX 309, subtractor 310, register 311.

23. In light of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, and to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Rubin proposes to testify that the term, "logic, coupled to the buffer memory, which monitors the transferring of data of a frame to the buffer memory to make a threshold determination of an amount of data of the frame transferred to the buffer memory," as it appears in claim 21 of U.S. Patent No. 5,434,872 and as disclosed in the specification under 35 U.S.C. § 112 ¶ 6, includes, without limitation: Figs. 11-12 – elements 300, 302, 303, 304, 305, 306, 307, 308, 309 310, 311, 320, 321, 322, and 323; Fig. 16 – elements 350, 351, 352, 353, 354, 355, 356, and 357.

24. In light of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, and to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Rubin proposes to testify that the term, "logic, responsive to the threshold determination of the logic which monitors the transferring of data to the buffer memory, which initiates transmission of the frame from the buffer memory to the medium access controller prior to transfer of all of the data of the frame to the buffer memory, including logic which initiates transmission of the frame when no complete frame of data is present in the buffer memory," as it appears in claim 21 of U.S. Patent No. 5,434,872 and as disclosed in the specification under 35 U.S.C. § 112 ¶ 6, includes, without limitation: Fig. 2 – threshold logic 36, threshold store 43; Fig. 3 – RAM 15; Fig. 5 – transmit descriptor and download DMA logic 107; Fig. 11 – counter 300, AND Gate 301, delay circuit 302, adder 304 and D-type flip-flops 305, 306; Fig. 12 – start threshold register 320, download compare block 321, immediate data comparator 322; Fig. 13 – threshold registers 330, 331, and threshold valid register 332; Fig. 14 – threshold valid state diagram elements 335-337; Fig. 15 –

comparator 340, AND gate 341, comparator 342; Fig. 16 – counter 350, comparators 351-353, MUX 354, and gate 355 comparator 357.

25. In light of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, and to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Rubin proposes to testify that the term, "means for comparing the counter to the threshold value in the alterable storage location," as it appears in claim 1 of U.S. Patent No. 5,307,459 and as disclosed in the specification under 35 U.S.C. § 112 ¶ 6, includes, without limitation: Fig. 2, includes without limitation – threshold logic 10, alterable storage location 10a, host processor 5, network adaptor 3; Figs. 12a-18, includes without limitation – register 221, counter 216, logic block 218, comparator 213, register 223, comparator 224, logic block 222; Figs. 19-23, includes without limitation. adder 317, comparator 318; Figs. 24-28, includes without limitation comparator 333; Figs. 29-34, includes without limitation, adder 614, comparator 615.

26. In light of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, and to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Rubin proposes to testify that the term, "network interface logic for transferring the data frame between the network transceiver and the buffer memory," as it appears in claim 1 of U.S. Patent No. 5,307,459 and as disclosed in the specification under 35 U.S.C. § 112 ¶ 6, includes, without limitation: Fig. 2 – network interface logic 11; Fig. 4 – receive DMA 63, Transmit DMA 67; Fig. 5 – network interface logic 104; Fig. 9 – transmit DMA logic 155; Fig. 11 – DMA logic 302; Figs. 14-18 – receive DMA Block; Figs. 29-34 – transmit DMA Block.

27. In light of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, and to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Rubin proposes to testify that the term, "host interface logic for transferring the data frame between the host system and the buffer memory," as it appears in claim 1 of U.S. Patent No. 5,307,459 and as disclosed in the specification under 35 U.S.C. § 112 ¶ 6, includes, without limitation: Fig. 2 – host interface logic 11; Fig. 4 – download DMA 58, upload DMA 57; Fig. 5 – host interface logic 102; Fig. 9 – host interface logic including 150 and 151; Fig. 11 – upload DMA logic 300 and preview logic 301; Figs. 19-23 – upload DMA Block; Figs. 24-28 – download DMA Block.

28. In light of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, and to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Rubin proposes to testify that the terms, "means … for transferring [data]" and "means, having a host system interface, for transferring data of frames to the buffer memory," as each of them appears in claim 1 of U.S. Patent No. 5,434,872 and as disclosed in the specification under 35 U.S.C. § 112 ¶ 6, include, without limitation: Fig. 1 – bus 2; Fig. 2 – host interface 31, bus 2; Fig. 3 – network interface processor 14, bus 13; Fig. 4 – RAM interface 50, host bus interface 51, EISA bus master interface 55, master slave union 53, download DMA module 57; Fig. 4A – download DMA module 58, download DMA offset bus [12:2], download DMA byte enable [3:0]; Fig. 5 – host interface logic 102, transmit descriptor and download DMA logic 107; Fig. 9 – host descriptor logic 150, download DMA logic 151, transmit descriptor ring buffer 152.

29. In light of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, and to the

extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Rubin proposes to testify that the terms, "means … for initiating [transmission]" and "means, responsive to the threshold determination of the means for monitoring, for initiating transmission of the frame prior to transfer of all the data of the frame to the buffer memory from the host computer," as each appears in claim 1 of U.S. Patent No. 5,434,872 and as disclosed in the specification under 35 U.S.C. § 112 ¶ 6, include, without limitation: Fig. 1 – early transmit logic 6A; Fig. 2 – transmit MAC logic; Fig. 3 – network interface processor; Fig. 4 & 4A – transmit DMA 67; Fig. 5 – network interface logic 104; Fig. 9 – transmit descriptor ring buffer 152, transmit DMA logic 155; Fig. 12 – data available control block 323; Fig. 17 – state machine elements 370, 371, 372, 373; Fig. 18 – transmit data path 400, data paths 401-402, MUX 410 and transmit control logic 411.

30. In light of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, and to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Rubin proposes to testify that the terms, "[host interface] means … for transferring [data]" and "host interface means, having an interface to the host system, for transferring data between the host system and the buffer memory," as each appears in claim 10 of U.S. Patent No. 5,434,872 and as disclosed in the specification under 35 U.S.C. § 112 ¶ 6, include, without limitation: Fig. 2 – host interface 31, bus 2; Fig. 3 – network interface processor 14, bus 13; Fig. 4 – RAM interface 50, host bus interface 51, EISA bus master interface 55, master slave union 53, upload DMA 57, download DMA module 58; Fig. 4A – download DMA module 58, download DMA offset bus [12:2], download DMA byte enable [3.0]; Fig. 5 – host interface logic 102, transmit descriptor logic and download DMA logic 107; Fig. 6 – transmit area; Fig. 7 – transmit descriptors; Fig. 9 – host descriptor logic 150, download DMA logic 151, transmit descriptor ring buffer 152; Fig. 11 – adder 308, MUX 309, subtractor 310, and register 311.

31. In light of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, and to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Rubin proposes to testify that the terms, "means … for monitoring [the transferring of data]" and "means, coupled with the buffer memory and including a host system alterable threshold store for storing a threshold value, for monitoring the transferring of data of a frame to the buffer memory to make a threshold determination of an amount of data of the frame transferred to the buffer memory," as each appears in claim 1 and claim 10, respectively, of U.S. Patent No. 5,434,872 and as disclosed in the specification under 35 U.S.C. § 112 ¶ 6, include, without limitation: Fig. 2 – threshold logic 36, threshold store 43; Fig. 3 – RAM 15; Fig. 5 – transmit descriptor and download DMA logic 107; Fig. 11 – counter 300, AND Gate 301, delay circuit 302, adder 304, and D-type flip-flops 305, 206; Fig. 12 – start threshold register 320, download compare clock 321, and immediate data comparator 322; Fig. 13 – threshold registers 330, 331, and threshold valid register 332; Fig. 14 – threshold value state diagram elements 335-37; Fig. 15 – comparator 340, AND gate 341, comparator 342; Fig. 16 – counter 350, comparators 351-353, MUX 354, and gate 355, comparator 357.

32. In light of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, and to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Rubin proposes to testify that the term, "means, responsive to the threshold determination of the means for monitoring, for initiating transmission of the frame, prior to transfer of all the data of the frame to the buffer memory from the host computer," as it appears in claim 1 of U.S. Patent No. 5,434,872 and as disclosed in the specification under 35 U.S.C. § 112 ¶ 6, includes, without limitation: Fig. 1 – early transmit logic 6A; Fig. 9 – transmit descriptor ring buffer 152, transmit DMA logic 155;

Fig. 12 – data available control block 323; Fig. 17 – state machine elements 370, 371, 372, 373; Fig. 18 – transmit data path 400, data paths 401-402, MUX 410 and transmit control logic 411.

33. In light of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, and to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Rubin proposes to testify that the terms, "[network interface] means … for transferring [data]" and "network interface means, having an interface to the network transceiver and responsive to the means for initiating, for transferring data between the buffer memory and the network transceiver for transmission," as each appears in claim 10 of U.S. Patent No. 5,434,872 and as disclosed in the specification under 35 U.S.C. § 112 ¶ 6, include, without limitation: Fig. 3 – network interface processor 14, encoder/decoder 19; Fig. 4 – cycle arbiter 56, interrupt controller 60, Ethernet transmitter 66, and transmit DMA 67; Fig. 4A – transmit DMA 67; Fig. 5 – transmit DMA Logic 109; Fig. 7 – transmit descriptors; Fig. 9 – transmit descriptor ring buffer 152, transmit DMA logic 155; Fig. 18 – transmit data path 400, data paths 401-402, MUX 410 and transmit control logic 411.

34. In light of the patent, prosecution history, and specification, in connection with his knowledge of how such terms are used by a person having ordinary skill in the art, and to the extent that the Court finds this element to be governed by 35 U.S.C. § 112 ¶ 6, Dr. Rubin proposes to testify that the terms, "[control] means … for posting [status information]" and "control means, coupled with the network interface means, for posting status information for use by the host system, as feedback for optimizing the threshold value," as each appears in claim 10 of U.S. Patent No. 5,434,872 and as disclosed in the specification under 35 U.S.C. § 112 ¶ 6, include, without limitation: Fig. 18 – transmit control logic 411 and underrun detector 413.

II. SUMMARY OF TESTIMONY OF NICK BAMBOS IN SUPPORT OF REALTEK'S POSITIONS SET FORTH IN THE JOINT CLAIM CONSTRUCTION AND PREHEARING STATEMENT PURSUANT TO PATENT LOCAL RULE 4-3

A. QUALIFICATIONS

Dr. Nick Bambos received his Ph.D. in Electrical Engineering and Computer Sciences in 1989, his M.S. degree in EECS in 1987, and his M.A. degree in Mathematics in 1989 all from the University of California at Berkeley.

Dr. Bambos is now a professor at Stanford University, having a joint appointment in the Department of Electrical Engineering and the Department of Management Science & Engineering. He heads the Network Architecture and Performance Engineering research group, comprised of doctoral students and research visitors conducting research in wireless network architectures, the Internet infrastructure, network security/reliability and operations management. His current research interests include high-reliability/security information systems, autonomic computing, and management of IP/wireless network infrastructures.

Dr. Bambos has held the Cisco Systems Faculty Development Chair in computer networking at Stanford from 1999 to 2003. He has also won the IBM Faculty Award in 2002 for high-impact research in performance engineering of computer systems and networks, as well as the Griffin Award in 1997. He has been the Morgenthaler Faculty Scholar at Stanford from 1996 to 1999. Dr. Bambos has also received the National Young Investigator Award in 1992 from the National Science Foundation (NSF) for research in computer networks and distributed computing architectures, as well as the NSF Research Initiation Award in 1990 for studies in performance modeling of computer systems.

Dr. Bambos has been a U.C. Regents Fellow, a David Gale Fellow, and an Earl Anthony Fellow, and is now on the Editorial Boards of several research journals and serves on various international technical committees and review panels for networking research and

information technologies.

B. GENERAL TESTIMONY

Dr. Bambos may be called to testify as Realtek's expert regarding the general purpose and use of network interface cards and Ethernet networking technology, as well as the specific network interface cards of the patents-in-suit. He may also testify as to the level of experience, knowledge, and skill typical of a person having ordinary skill in those arts concerned with the technology disclosed in the patents-in-suit and how the terms proposed collectively by both sides in this action for construction are used by a person having ordinary skill in the art, and specifically how such a person would interpret such terms in the context of the respective specifications, claims, and prosecution histories of the patents-in-suit. Dr. Bambos may also testify as to the structure(s), act(s), and/or material(s), and equivalents or lack thereof, disclosed in the respective specifications of the patents-in-suit or known to a person having ordinary skill in the art for each claim element found by the court to be governed by 35 U.S.C. § 112(6).

C. TESTIMONY ON CLAIM CONSTRUCTION

Dr. Bambos is also expected to provide written or oral testimony on the following matters:

1. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term, "buffer," as it appears in claims 23 of U.S. Patent No. 6,327,625 and claim 1 of U.S. Patent No. 6,570,884, to mean "a temporary storage area in random access memory where the NIC or computer stores information."

2. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term, "logic," as it appears in claim 23 of U.S. Patent No. 6,327,625 and claim 1 of U.S. Patent No. 6,570,884 to mean "a device," should the Court determine that the term should not be construed under 35 U.S. C. § 112 ¶ 6.

3. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term, "order of receipt," as it appears in claim 23 of U.S. Patent No. 6,327,625, to mean "the order in which the packets are received by the buffer."

4. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term, "packet types," as it appears in claim 23 of U.S. Patent No. 6,327,625, to mean "packets with different formats or priorities."

5. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term, "transfer packets out of the buffer to the other of the first and second ports according to the order of receipt, and according to the respective packet types," as it appears in claim 23 of U.S. Patent No. 6,327,625, to mean "the order in which packets are transferred out of the buffer is based upon the order in which the packets were received by the buffer and the types of the packets stored in the buffer."

6. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term, "data download circuit," as it appears in claim 26 of U.S. Patent No. 6,526,446, to mean "the circuitry that downloads data corresponding to the frame segment descriptor."

7. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term, "descriptor signal," as it appears in claim 26 of U.S. Patent No. 6,526,446, to mean "a signal indicating where the corresponding data is in the host memory."

8. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term, "frame segment descriptor," as it appears in

claim 26 of U.S. Patent No. 6,526,446, to mean "a descriptor identifying where the corresponding frame segment is in the host memory."

9. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term, "first logic," as it appears in claim 1 of U.S. Patent No. 6,570,884 to mean "first device," should the Court determine that the term should not be construed under 35 U.S. C. § 112 ¶ 6.

10. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term, "read and process data in the identified packets from the buffer," as it appears in claim 1 of U.S. Patent No. 6,570,884, to mean "read and process data in the identified packets while the packets are in the buffer."

11. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term, "second logic," as it appears in claim 1 of U.S. Patent No. 6,570,884 to mean "second device," should the Court determine that the term should not be construed under 35 U.S. C. § 112 ¶ 6.

12. In light of the patent, prosecution history, and specification, a person having ordinary skill in the art would understand the term, "variant formats," as it appears in claim 1 of U.S. Patent No. 6,570,884, to mean "differing formats."

EXHIBIT C